DATA SHEET

GPCV2159A

Vehicle Camera Recorder SoC Solution

Preliminary

Nov. 10, 2014

Version 0.2

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VEHICLE CAMERA RECORDER SoC SOLUTION

1. GENERAL DESCRIPTION

The GPCV2159A, a highly integrated SoC processor for vehicle camera recorder, is based on a high performance and power efficient ARM1176JZFS core operating at up to 702MHz and is enhanced with image, video processing, power saving, and system peripherals.

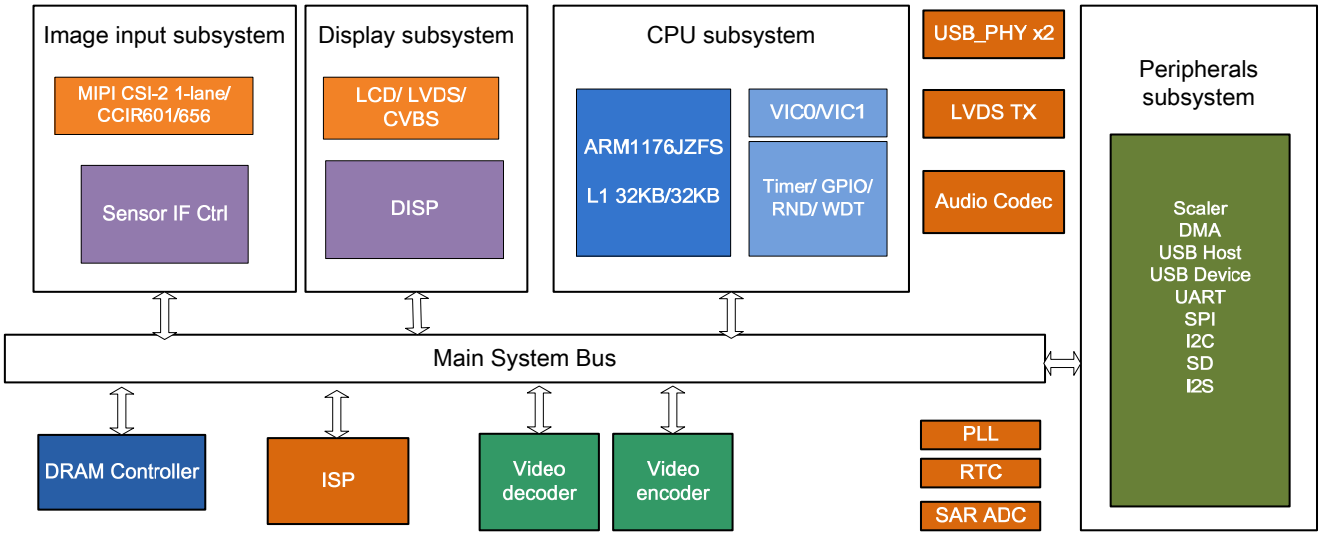
The high-speed MJPEG engine is capable of supporting video compression up to 1080p/30fps. Other main features include a high-performance Image Signal Processing (ISP) hardware-accelerating pipeline to boost the conventional raw-data CMOS sensor up to 5M pixels and an HDMI Tx for HDTV output to deliver high-resolution graphics. ARM1176JZFS processor is designed to connect with various types of memory card interfaces such as SD, SDHC, SDIO, and MMC.

These fully featured peripherals and functions make GPCV2159A one of the best vehicle camera SoC solutions in the industry- making your products more competitive in today's market.

2. FEATURES

- High performance CPU + HW video codec architecture
- ARM1176JZFS CPU with 32KB I-cache and 32KB D-cache, Vector Floating Point (VFP) Coprocessor, embedded JTAG ICE, and working frequency up to 600MHz
- HW video decoder. Supports JPEG/MJPEG/MPEG4 SP/ASP, H.263, H.264 BP/MP/HP. All format support up-to 1080p resolution.
- HW video encoder. Supports JPEG/MJPEG (max. 4672x3504 size), H.264 BP/MP/HP up-to 1080P 30fps/720P 60fps.
- Video-in & CMOS sensor interface, Two single-lane MIPI sensor interface (max. 768Mbps data rate, only one can active at the same time) and CCIR601/ CCIR656 standard support
- Image signal processing hardware-accelerating pipeline
- High quality scalar engine
- AES-128 encryption and decryption
- Display engine
  - TFT-LCD controller
    - UPS051 / UPS052 (serial RGB)
    - Parallel RGB (5-6-5, 6-6-6, 8-8-8)
    - I80 (8-bit/16-bit system bus) I/F type
    - CCIR601/CCIR656
    - Digital Timing Controller for TFT-LCD drivers
  - TV encoder with VDAC output
    - NTSC/PAL output
    - De-flicker function
  - Real time OSD, which also supports OSD scaling up
  - Real time (on screen) scalar engine inside to fit the display screen
  - Programmable RGB gamma correction
  - Color convert matrix for display
  - Built-in 1-channel LVDS transmitter. Support RGB666/ RGB888 up-to 1366x768 resolution
- Watchdog timer
- Real-time clock
- Programmable general I/O ports (GPIO) with pull-high/low control
- Two USB_PHY interface with one built-in USB device controller and two USB EHCI/OHCI host controllers. Both USB_PHY can switch to host or device controller.
- UART interface with baud rate up to 1.8432Mbps and 115.2Kbps
- SPI (master) interface
- I2C interface
- I2S master/slave
- SD/SDHC/SDIO/MMC card interface, which also supports eMMC interface
- Stereo Sigma/Delta DAC for audio playback
- Stereo line-in and Microphone line-in for audio recorder
- 10-bit ADC with 5 line-in channels, which also supports Touch panel application
- BGA224 package

3. BLOCK DIAGRAM



4. PIN DESCRIPTIONS

Pin No.	BALL Number	Pin name	Pin Description
1	D2	ADAC_OUTR	Right channel audio output
2	D1	ADAC_OUTL	Left channel audio output
3	K7	AVDD3V3_ACODEC	3.3V Audio CODEC power
4	K6	AVSS_ACODEC	Audio CODEC ground
5	H6	ADAC_VREF	Audio CODEC reference voltage
6	E2	LINEINR	Right channel line in
7	E1	LINEINL	Left channel line in
8	F2	MIC_IN	Microphone input
9	F1	MIC_BIAS	Microphone bias
10	G2	IOC15	SPK Mute
11	G1	IOC14	AHP Sense
12	H2	IOC13	
13	H1	IOC12	Shot Key
14	J2	IOC11	Record Key
15	J1	IOC10	Mode Key
16	K2	IOC9	
17	K1	IOC8	
18	L2	IOB7	
19	L1	IOB6	
20	M2	IOB5	
21	M1	IOB4	
22	N2	IOB3	
23	N1	IOB2	
24	P2	IOB1	LCD SCL
25	P1	IOB0	LCD SDA
26	R2	IOD10	LCD Data 7
27	L6	IOD9	LCD Data 6
28	M7	IOD8	LCD Data 5
29	M6	IOD7	LCD Data 4
30	N7	IOD6	LCD Data 3
31	N6	IOD5	LCD Data 2
32	P7	IOD4	LCD Data 1
33	P6	IOD3	LCD Data 0/IOTRAP
34	R7	IOA15	LCD CE
35	R6	IOD2	LCD HSYNC
36	P8	IOD1	LCD VSYNC
37	R8	IOD0	LCD CLK
38	Y2	IOC7	LCD BL EN
39	W1	IOC6	
40	Y3	IOC5	
41	Y1	IOC4	
42	W2	IOC3	
43	V1	IOC2	Sensor Reset
44	W3	IOC1	PWR Key Det

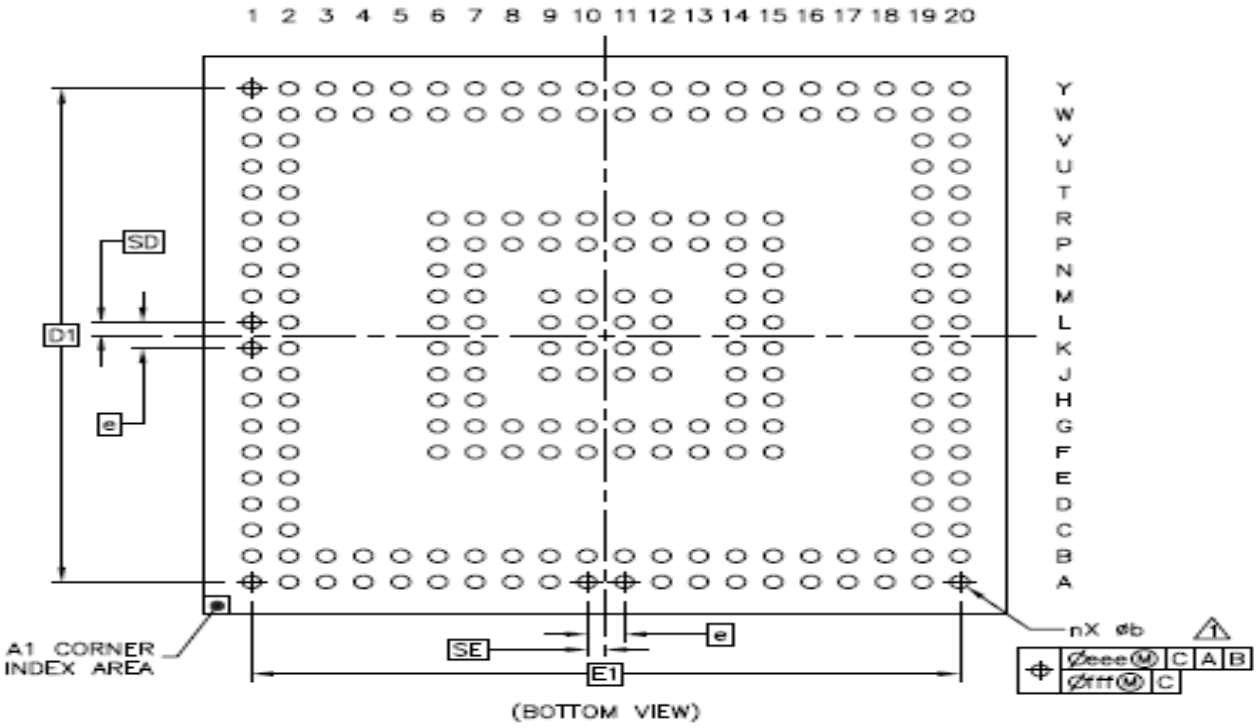
Pin No.	BALL Number	Pin name	Pin Description
45	U1	IOC0	PWR EN
46	U2	IOA13	
47	T1	IOA12	
48	T2	IOA11	
49	R1	IOA10	Sensor MIPI MCLK
50	V2	IOA14	
51	Y4	IOC27	Sensor MIPI CLKP
52	W4	IOC26	Sensor MIPI CLKN
53	Y5	IOC25	Sensor MIPI DATA0P
54	W5	IOC24	Sensor MIPI DATA0N
55	W6	IOB20	
56	Y7	IOB21	
57	Y6	IOB22	
58	W7	IOB23	
59	W8	IOB24	
60	Y8	IOB25	
61	Y9	HDMI_TXCN	HDMI_TXCN
62	W9	HDMI_TXCP	HDMI_TXCP
63	Y10	HDMI_TXN0	HDMI_TXN0
64	W10	HDMI_TXP0	HDMI_TXP0
65	Y11	HDMI_TXN1	HDMI_TXN1
66	W11	HDMI_TXP1	HDMI_TXP1
67	Y12	HDMI_TXN2	HDMI_TXN2
68	W12	HDMI_TXP2	HDMI_TXP2
69	R9	AVSS_HDMI	AVSS_HDMI
70	R11	AVDD1V2_HDMI	AVDD1V2_HDMI
71	L7	AVDD3V3_HDMI_VDAC	AVDD3V3_HDMI_VDAC
72	R12	VDAC_OUT0	VDAC_OUT0
73	R10	VDAC_RSET	VDAC_RSET
74	R13	VDAC_CBU	VDAC_CBU
75	P12	VDD3V3_DRAM_PLL	VDD3V3_DRAM_PLL
76	P13	DRAM_VREF	DRAM_VREF
77	L19	VSS_PWM	VSS_PWM
78	L20	PWM0_PWM	
79	K19	PWM1_PWM	
80	J19	IOD25	
81	K20	IOD26	
82	J20	IOD27	LCD BL ADJ
83	P20	IOE6	
84	M20	IOE5	
85	N19	IOE3	
86	N20	IOE4	
87	P19	IOE8	
88	M19	IOE7	
89	H19	IOD11	

Pin No.	BALL Number	Pin name	Pin Description
90	H20	IOD12	
91	G19	IOD13	
92	F19	IOD14	
93	G20	IOD15	
94	E19	IOD16	
95	F20	IOD17	
96	E20	IOD18	
97	D19	IOD19	
98	D20	IOD20	
99	C19	IOD21	
100	C20	IOD22	
101	B20	IOD23	UP Key
102	B19	IOD24	Down Key
103	A20	IOA20	GPS PWR EN
104	A19	IOA21	SDC PWR EN
105	A15	IOE0	Battery Det
106	B16	IOE1	Battery Det Ref
107	A16	IOE2	
108	B17	IOA19	LED
109	A17	IOA18	IR LED EN
110	B18	IOA17	Sensor PWR EN
111	A18	IOA16	
112	B13	IOB19	UART RX
113	A13	IOB18	UART TX
114	B15	IOA22	USB Det
115	A14	IOA29	HDMI HP
116	B14	IOA30	GPS Rcv
117	B12	IOB16	HDMI/Gsensor I2C SDA
118	A12	IOB17	HDMI/Gsensor I2C SCL
119	A11	IOA7	SPI Flash CLK
120	B11	IOA6	SPI Flash RX
121	A10	IOA5	SPI Flash TX
122	B10	IOA4	SPI Flash CS0
123	A9	IOA3	Gsensor INT
124	B9	IOA2	SDC Det
125	A8	IOA1	Sensor I2C SDA
126	B8	IOA0	Sensor I2C SCL
127	A7	IOA26	SD0_D1
128	A5	IOA25	SD0_D0
129	B7	IOA23	SD0_CLK
130	B5	IOA24	SD0_CMD
131	A6	IOA28	SD0_D3
132	B6	IOA27	SD0_D2
133	F9	TEST_XTAL	Connect to VDD3V3
134	A4	USB1_DM	USB high speed D-

Pin No.	BALL Number	Pin name	Pin Description
135	B4	USB1_DP	USB high speed D+
136	F8	AVSS_USB1	USB1 ground
137	G8	AVDD3V3_USB1_USB0	3.3V USB power
138	A3	USB0_DM	
139	B3	USB0_DP	
140	F7	AVSS_USB0	USB0 ground
141	F6	VDD3V3_RTC	RTC power
142	G6	RTCINT33	RTC INT output
143	A2	XTAL_32K_IN	XTAL_32K_IN
144	B2	XTAL_32K_OUT	XTAL_32K_OUT
145	G7	VSS_RTC_XTAL	RTC and XTAL ground
146	A1	XTAL_27M_IN	27M XTAL PAD
147	B1	XTAL_27M_OUT	27M XTAL PAD
148	J7	A3V3_XTAL_APLL	A3V3 XTAL + APLL power
149	H7	VSS_APLL_PLL	APLL and PLL ground
150	J6	VDD1V2_PLL_XTAL_APLL	1.2V PLL/APLL/XTAL power
151	C1	TEST	TEST mode enable, tie 0
152	C2	RESETB	Super reset, active low
153	N15	NC	NC
154	P14	NC	NC
155	P15	NC	NC
156	R14	NC	NC
157	R15	NC	NC
158	J10	VSS_CORE	Core ground
159	J11	VSS_CORE	Core ground
160	J12	VSS_CORE	Core ground
161	K10	VSS_CORE	Core ground
162	K11	VSS_CORE	Core ground
163	K12	VSS_CORE	Core ground
164	L9	VSS_CORE	Core ground
165	L10	VSS_CORE	Core ground
166	L11	VSS_CORE	Core ground
167	M9	VSS_CORE	Core ground
168	M10	VSS_CORE	Core ground
169	M11	VSS_CORE	Core ground
170	P9	VSS_CORE	Core ground
171	P10	VSS_CORE	Core ground
172	P11	VSS_CORE	Core ground
173	F14	VDD1V2_CORE	1.2V Core power
174	F15	VDD1V2_CORE	1.2V Core power
175	G14	VDD1V2_CORE	1.2V Core power
176	G15	VDD1V2_CORE	1.2V Core power
177	H14	VDD1V2_CORE	1.2V Core power
178	H15	VDD1V2_CORE	1.2V Core power
179	J14	VDD1V2_CORE	1.2V Core power

Pin No.	BALL Number	Pin name	Pin Description
180	J15	VDD1V2_CORE	1.2V Core power
181	K14	VDD1V2_CORE	1.2V Core power
182	K15	VDD1V2_CORE	1.2V Core power
183	L12	VDD1V2_CORE	1.2V Core power
184	L14	VDD1V2_CORE	1.2V Core power
185	L15	VDD1V2_CORE	1.2V Core power
186	M12	VDD1V2_CORE	1.2V Core power
187	M14	VDD1V2_CORE	1.2V Core power
188	M15	VDD1V2_CORE	1.2V Core power
189	N14	VDD1V2_CORE	1.2V Core power
190	W13	VDD_DRAM_IO	DRAM IO Power (1.5V)
191	W14	VDD_DRAM_IO	DRAM IO Power (1.5V)
192	W15	VDD_DRAM_IO	DRAM IO Power (1.5V)
193	W16	VDD_DRAM_IO	DRAM IO Power (1.5V)
194	W17	VDD_DRAM_IO	DRAM IO Power (1.5V)
195	W18	VDD_DRAM_IO	DRAM IO Power (1.5V)
196	Y13	VDD_DRAM_IO	DRAM IO Power (1.5V)
197	Y14	VDD_DRAM_IO	DRAM IO Power (1.5V)
198	Y15	VDD_DRAM_IO	DRAM IO Power (1.5V)
199	Y16	VDD_DRAM_IO	DRAM IO Power (1.5V)
200	Y17	VDD_DRAM_IO	DRAM IO Power (1.5V)
201	Y18	VDD_DRAM_IO	DRAM IO Power (1.5V)
202	R19	VSS_DRAM_IO	DRAM IO GND
203	R20	VSS_DRAM_IO	DRAM IO GND
204	T19	VSS_DRAM_IO	DRAM IO GND
205	T20	VSS_DRAM_IO	DRAM IO GND
206	U19	VSS_DRAM_IO	DRAM IO GND
207	U20	VSS_DRAM_IO	DRAM IO GND
208	V19	VSS_DRAM_IO	DRAM IO GND
209	V20	VSS_DRAM_IO	DRAM IO GND
210	W19	VSS_DRAM_IO	DRAM IO GND
211	W20	VSS_DRAM_IO	DRAM IO GND
212	Y19	VSS_DRAM_IO	DRAM IO GND
213	Y20	VSS_DRAM_IO	DRAM IO GND
214	F10	VDD3V3_IO	3.3V IO power
215	F11	VDD3V3_IO	3.3V IO power
216	F12	VDD3V3_IO	3.3V IO power
217	F13	VDD3V3_IO	3.3V IO power
218	G9	VDD3V3_IO	3.3V IO power
219	G10	VDD3V3_IO	3.3V IO power
220	G11	VDD3V3_IO	3.3V IO power
221	G12	VDD3V3_IO	3.3V IO power
222	G13	VDD3V3_IO	3.3V IO power
223	J9	VDD3V3_IO	3.3V IO power
224	K9	VDD3V3_IO	3.3V IO power

4.1. Pin Map


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Y
W
V
U
T
R
P
N
M
L
K
J
H
G
F
E
D
C
B
A
SD
D1
e
A1 CORNER INDEX AREA
SE
e
E1
nX øb
(BOTTOM VIEW)

5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Rating

Rating	Symbol	Value	Unit
Supply Voltage 1	VDD3V3_IO_LVDS VDD3V3_IO_MIPI VDD3V3_DRAM_PLL VDD3V3_IO_PWM VDD3V3_IO A3V3_XTAL_APLL AVDD3V3_ACODEC AVDD3V3_VDAC AVDD3V3_IO_ADC AVDD3V3_USB1_USB0	-0.3 to 3.6	V
Supply Voltage 2	VDD1V2_CORE VDD1V2_CORE_MIPI VDD1V2_DRAM_CORE VDD1V2_PLL_XTAL_APLL	-0.3 to TBD	V
Supply Voltage 3	VDD_DRAM_IO	-0.3 to 2.75	V
Supply Voltage 4	VDD3V3_RTC	-0.3 to 3.6	V
Input Voltage	V_{IN}	-0.3 to 3.6	V
Operating Temperature	T_A	-40 to 70	℃
Storage Temperature	T_{STG}	-40 to +150	℃

5.2. DC Characteristics

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage 1	VDD3V3_IO_LVDS VDD3V3_IO_MIPI VDD3V3_DRAM_PLL VDD3V3_IO_PWM VDD3V3_IO A3V3_XTAL_APLL AVDD3V3_ACODEC AVDD3V3_VDAC AVDD3V3_IO_ADC AVDD3V3_USB1_USB0	3.0	3.3	3.6	V	-
Operating Voltage 2	VDD1V2_CORE VDD1V2_CORE_MIPI VDD1V2_DRAM_CORE VDD1V2_PLL_XTAL_APLL	1.2	-	1.32	V	-
Operating Voltage 3	VDD_DRAM_IO (DDR3)	1.35	1.5	1.65	V	-
	VDD_DRAM_IO (mDDR/DDR2)	1.62	1.8	1.98	V	-
	VDD_DRAM_IO (DDR)	2.25	2.5	2.75	V	-
Operating Voltage 4	VDD3V3_RTC	TBD	3.3	TBD	V	-
Input High Voltage	V_{IH}	2	-	3.6	V	Based on 3.3V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V	Based on 3.3V

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Output High Driving Current (4mA setting)	GPIO I_{oH}	-	5.1	-	mA	VOH=2.4V, VDD3V3_IO=3.3V
Output Low Driving Current (4mA setting)	GPIO IO I_{oH}	-	4.1	-	mA	VOL=0.4V, VDD3V3_IO=3.3V
Output High Driving Current (8mA setting)	GPIO I_{oH}	-	10	-	mA	VOH=2.4V, VDD3V3_IO=3.3V
Output Low Driving Current (8mA setting)	GPIO IO I_{oH}	-	8.1	-	mA	VOL=0.4V, VDD3V3_IO=3.3V
Pull-up resistor	Rpu	-	53K	-	Ohm	VDD3V3_IO=3.3V
Pull-down resistor	Rpd	-	51K	-	Ohm	VDD3V3_IO=3.3V
Sleep mode current	I_{sleep}	-	-	66	mA	All clock and all macros turn off
Core Power Normal current 1	$I_{core\_normal1}$	-	355	-	mA	ARM@594MHz, SYS/H.264 encode 1080p@297MHz; DDR3 memory@297MHz VDD1V2_CORE=1.32V
DDR Normal current 1	I_{ddr1}	-	136	-	mA	ARM@594MHz, SYS/H.264 encode 1080P@297MHz; DDR3 memory@297MHz VDD_DRAM_IO=1.5V
Core Power Normal current 2	$I_{core\_normal2}$	-	186	-	mA	ARM@400MHz, SYS@162MHz; DDR3 memory@162MHz VDD1V2_CORE=1.2V Flashplayer with OVG engine.
DDR Normal current 2	I_{ddr2}	-	63	-	mA	ARM@400MHz, SYS@162MHz; DDR3 memory@162MHz VDD_DRAM_IO=1.5V Flashplayer with OVG engine.
Crystal Frequency 1	-	-	32768	-	Hz	-
Crystal Frequency 2	$F_{CRYSTAL}$	-	27.0[1]	-	MHz	-

5.3. Video DAC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	-	9	10	Bit	Rset=390Ohm ,Load=37.5Ohm
INL	-	±1.3	-	LSB	-
DNL	-	±0.3	-	LSB	-
Voltage Reference Range	1.14	1.235	1.33	V	-

5.4. Stereo Audio DAC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	-	-	20	Bit	-
Full Scale Output Voltage	-	1.0	-	Vp-p	-
SNR	-	98	-	dB	Fin=0.997KHz, Fs=48kHz, R_L=100KOhm,

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
					AVDD3V3_ACODEC=3.3V
THD+N	-	85	-	dB	Fin=0.997KHz, Fs=48kHz, RL=100KOhm, AVDD3V3_ACODEC=3.3V
Dynamic Range	-	96	-	dB	Fin=0.997KHz, Fs=48kHz, RL=100KOhm, AVDD3V3_ACODEC=3.3V
Output Loading	100	-	-	ohm	-
Frequency Response	20	-	20K	Hz	-

5.5. Stereo Audio ADC/MIC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	-	-	16	Bit	-
Input Voltage Range	3.0	-	3.6	V	-
SNR	-	84	-	dB	Fin=0.997KHz, Fs=48kHz, AVDD3V3_ACODEC=3.3V
THD+N	-	80	-	dB	Fin=0.997KHz, Fs=48kHz, AVDD3V3_ACODEC=3.3V
Dynamic Range	-	83.5	-	dB	Fin=0.997KHz, Fs=48kHz, AVDD3V3_ACODEC=3.3V
VREF	-	1.63	-	V	-

5.6. SAR ADC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	-	-	10	bits	-
SAR ADC Input Voltage Range	3.0	-	3.6	V	-
SINAD	-	55	-	dB	ADC clock=768KHz, Fs=48KHz, AVDD3V3_IO_ADC=3.3V
Effective Number of Bit	-	9	-	bits	-
INL	-	±0.6	-	LSB	-
DNL	-	±0.6	-	LSB	-
AD Conversion Rate	-	-	125K	Hz	-

5.7. PWM Characteristics

Characteristics	Conditions	Symbol	Min.	Typ.	Max.	Unit
V_{33_IO} Operating Current	-	PWM0_PWM, PWM1_PWM	-	0.5	-	mA
V_{33_AD} Operating Current	-	PWM0_FB, PWM1_FB, PWM1_VC1	-	0.185	-	mA
PWM0 Switching Frequency	-	fPWM0	-	600	-	kHz
PWM0 Internal Reference Voltage	-	-	-	1.250	-	V
PWM1 Switching Frequency	-	fPWM1	-	600	-	kHz

Characteristics	Conditions	Symbol	Min.	Typ.	Max.	Unit
PWM1 Internal Reference Voltage	VSET[3:0]=0000	-	-	25	-	mV
	VSET[3:0]=0001	-	-	50	-	mV
	VSET[3:0]=0010	-	-	75	-	mV
	VSET[3:0]=0011	-	-	100	-	mV
	VSET[3:0]=0100	-	-	125	-	mV
	VSET[3:0]=0101	-	-	150	-	mV
	VSET[3:0]=0110	-	-	175	-	mV
	VSET[3:0]=0111	-	-	200	-	mV
PWM1 Internal Reference Voltage	VSET[3:0]=1000	-	-	225	-	mV
	VSET[3:0]=1001	-	-	250	-	mV
	VSET[3:0]=1010	-	-	275	-	mV
	VSET[3:0]=1011	-	-	300	-	mV
	VSET[3:0]=1100	-	-	325	-	mV
	VSET[3:0]=1101	-	-	350	-	mV
	VSET[3:0]=1110	-	-	375	-	mV
	VSET[3:0]=1111 (default)	-	-	400	-	mV

6. PACKAGE/PAD LOCATION

6.1. Ordering Information

Product Number	Package Type
GPCV2159A- NnnV - QBM1x	Halogen Free Package

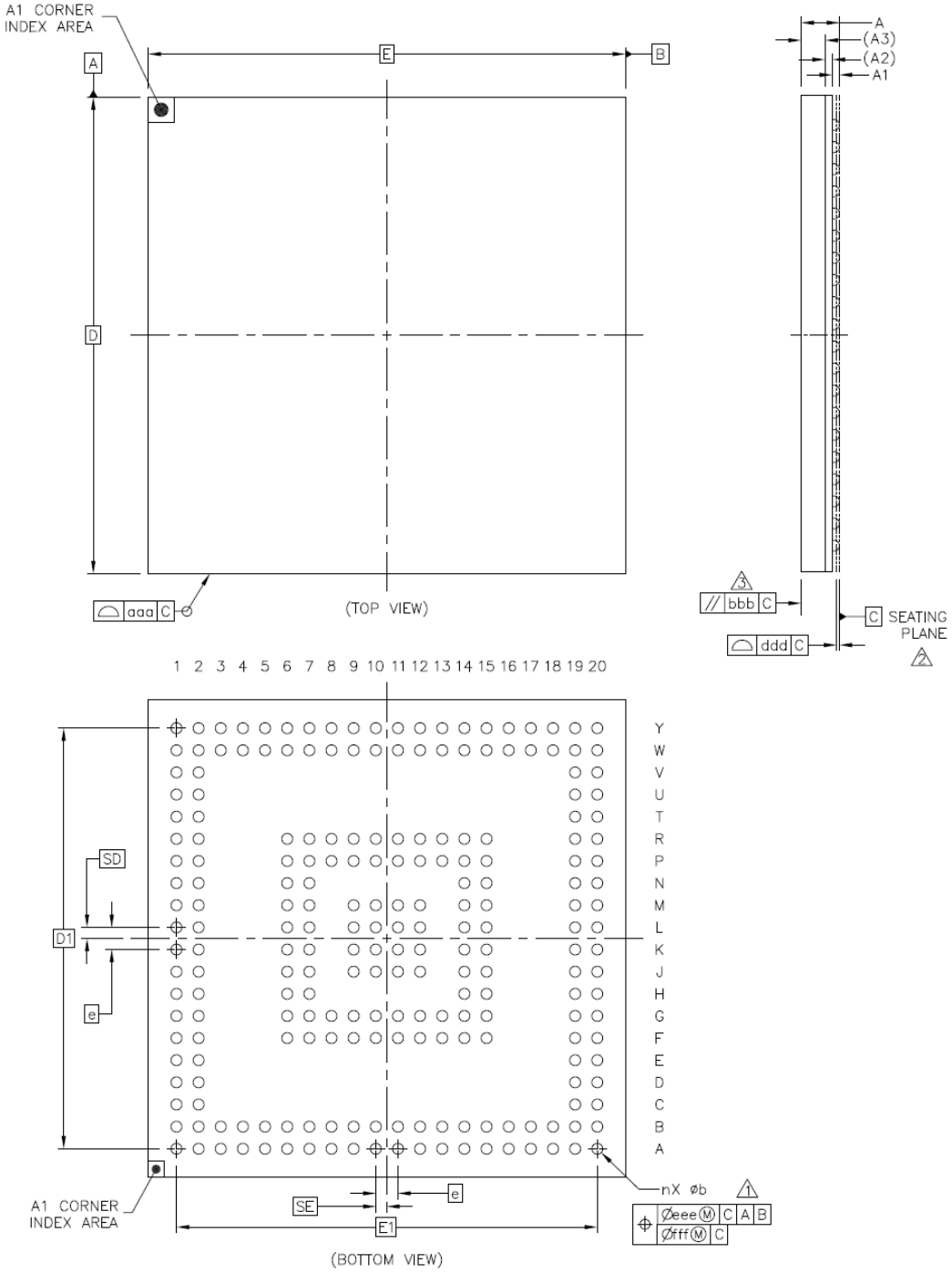
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

6.2. Package Information

BGA224



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.2
STAND OFF	A1	0.16	---	0.26
SUBSTRATE THICKNESS	A2		0.21	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		14	BSC
	E		14	BSC
BALL DIAMETER			0.3	
BALL OPENING			0.275	
BALL WIDTH	b	0.27	---	0.37
BALL PITCH	e		0.65	BSC
BALL COUNT	n		224	
EDGE BALL CENTER TO CENTER	D1		12.35	BSC
	E1		12.35	BSC
BODY CENTER TO CONTACT BALL	SD		0.325	BSC
	SE		0.325	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

7. DISCLAIMER

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8. REVISION HISTORY

Date	Revision #	Description	Page
Nov 10, 2014	0.2	Modify CPU max. frequency , MJPEG frame rate and MIPI data rate.	3
Sep 02, 2014	0.1	Preliminary version	18