DATA SHEET

GPM4730A

Cortex M4F Multi-media Video Streaming SoC Platform

Preliminary

Mar. 03, 2016

Version 0.1

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MULTI-MEDIA VIDEO STREAMING SoC PLATFORM

1. GENERAL DESCRIPTION

GPM4730A, a highly integrated SoC (System-On a Chip) by Generalplus, is a high cost-performance ratio solution for multi-media and video streaming applications. It is developed with a high performance and power efficient ARM's Cortex M4F core operating at up to 193.5MHz with significant enhancements in image, video processing, and power savings. Other features include DDR memory, 720p30 H.264/JPEG CODEC engine, HD 720p HDMI interface, TFT-LCD interface, CMOS sensor interface, MIPI CSI interface, scaling engine, Picture Process Unit (PPU), 16-channel Sound Process Unit (SPU), USB 2.0 OHCI/EHCI, USB 2.0 HS device, etc. GPM4730A processor is designed to connect with various types of memory card interfaces such as SD and MMC. For more information about its features, please refer to the following section.

These fully featured peripherals and functions make GPM4730A one of the best multimedia-processor SoC solutions in the industry- making your products more competitive in today's market.

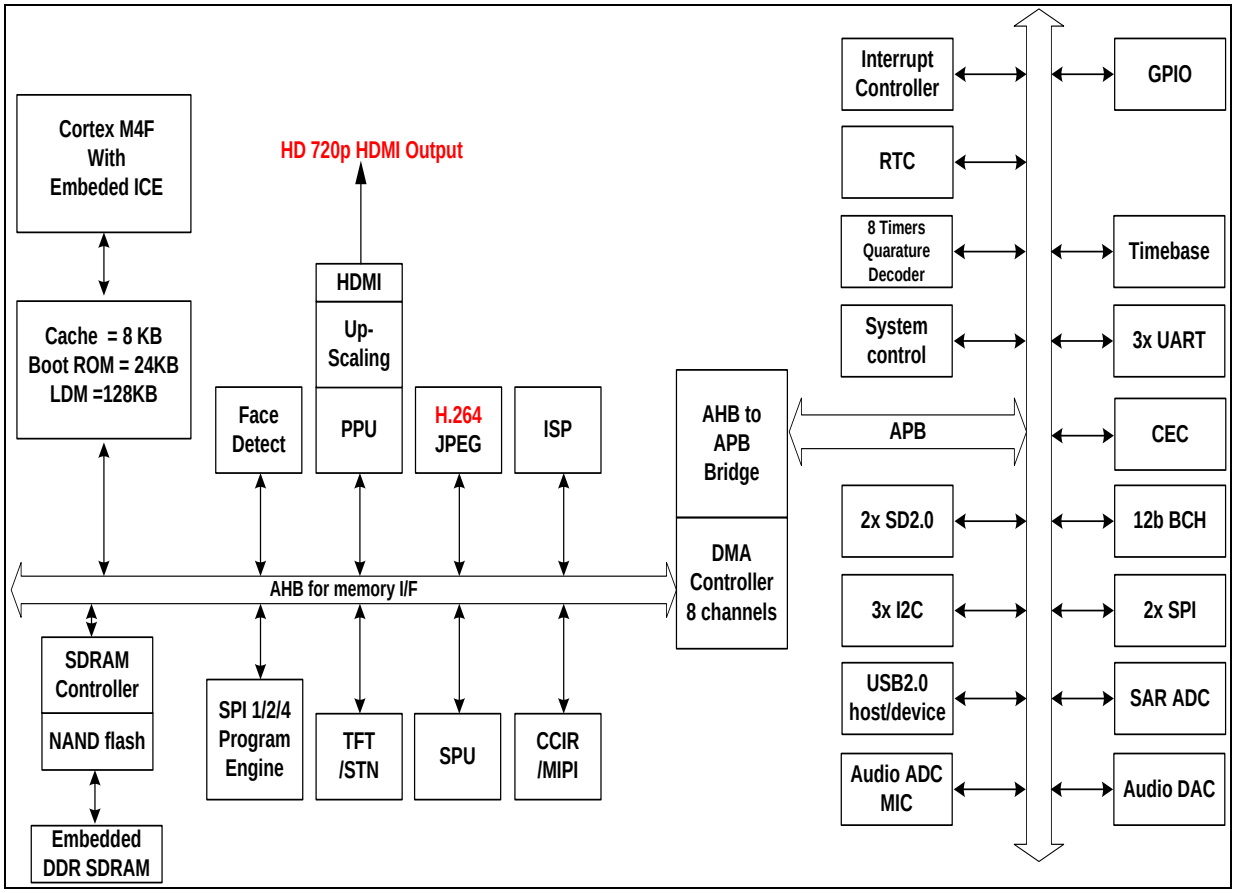
2. FEATURES

- ARM's Cortex M4F CPU with 8K-byte unified ID-cache, floating point co-processor, write buffer, embedded JTAG/SWD ICE, and working frequency up to 193.5MHz.
- 128KB SRAM for local data buffer.
- Embedded 256Mb DDR SDRAM.
- SPI Flash controller which CPU can run program directly on it. Supports 1-bit/2-bit/4-bit IO mode.
- Picture Process Unit. (PPU)
  - 4 Text layers + 1024 internal Sprites + 4096 extended Sprites.
  - Virtual 3D effect for text and sprite.
  - QVGA/VGA/D1 output.
  - Line-based or frame-based operation.
  - Max. 1024x768 LCD Resolution output.
  - Texture mapping with anti-aliasing and bilinear interpolation.
- Sound Process Unit. (SPU)
  - 16 hardware PCM/ADPCM channels.
  - Built-in dynamic volume compressor.
- JPEG CODEC.
  - ISO/IEC 10918-1 baseline JPEG.
  - High-speed decoding and encoding with resolution up to 64MPixel.
  - Hardware Motion JPEG decoding and encoding (up to 720p@30fps) for real-time video record and playback application.
- H.264 CODEC
  - H.264 baseline profile CODEC
  - Up-to 720p30 for real-time video record and playback application.
- Video-in & CMOS sensor interface and CCIR601/CCIR656 CSI standard supported.
- One set of 2-lane or two sets of 1-lane MIPI CSI input supported
- Face Detection Engine for interactive application.
- NAND FLASH controller with ECC and 4/8/12-bit BCH
- 1/2/4-bit SPI flash controller, capable of running program on SPI directly.
- Eight-channel DMA controller with AES/DES/3DES function.
- 720p HDMI output with VGA to 720p up-scaling engine.
- Mono and 16 gray levels STN-LCD controller.
- Rotating engine supports 90/180/270/360/Mirror/Flip function
- TFT-LCD controller.
  - UPS051. (serial RGB)
  - UPS052. (serial RGB dummy)
  - Parallel RGB (6-6-6, 7-7-7, 8-8-8).
  - I80 (8-bit/16-bit/18-bit system bus) I/F type.
  - CCIR601/CCIR656.
  - Built-in Timing Controller for TFT-LCD drivers.
  - Scaling engine inside with programmable up-scaling and down-scaling factor.
- Embedded ISP (Image Processing Unit), supports raw data sensor up to 5M pixels
  - Histogram statistics for auto brightness and contrast.
  - Programmable RGB gamma correction.
  - Color conversion matrix for various post-image processing.
  - WDR
  - Sharpen
  - De-noise
  - Bad-pixel cancelation
- Universal Serial Bus (USB) 2.0 high/full speed compliance device and USB OHCI/EHCE host controller with built-in transceiver.
- Watchdog timer.
- Real-time clock.
- Eight 32-bit timers/counters with PWM output capability.

- Eight channels quadrature decoder.
- Two sets of SD 2.0/MMC interface.
- Two sets of SPI (master/slave) interface with data rate up to 24Mbps.
- Three sets of UART (asynchronous serial I/O) or IrDA interface with baud rate up to 1.8432Mbps and 115.2Kbps. Smart card interface (ISO7816) is also supported.
- Three sets of I2C controller.
- CEC controller.
- Four sets of I2S input with 24-bit resolution and up to 192KHz sample rate.
- Four sets of I2S output with 24-bit resolution and up to 192KHz sample rate.
- 72 general programmable I/O ports (GPIO) with pull-high/low control.
- Power management
- Built-in 3.3V to 1.2V regulator for core logic.
- Built-in 3.3V to 2.8V regulator for sensor's power.
- Built-in 3.3V to 2.5V regulator for DDR memory.
- Low voltage reset.
- RTC with independent power supply.
- Fast boot from power-down mode with boot time less than 1ms.
- Power-down mode with low standby current, typically less than 20uA.
- Programmable PLL frequency from 12MHz to 193.5MHz.
- 16-bit stereo DAC (2-channel) for audio playback.
- 16-bit stereo ADC with MIC and LINEINR/LINEINL for audio recording.
- 12-bit SAR ADC with 3 line-in channels and 100Ksps.
- MIC with digital AGC (auto gain control)
- LQFP128 package

Item	Product number	Embedded DDR density
1	GPM4730A	256Mb DDR memory

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTION

PKG No	Name	Group	Type	Normal Function Description
1	V33_RTC	RTC	P	RTC power input
2	X32KI	RTC	AI	X'tal 32768Hz input
3	X32KO	RTC	AO	X'tal 32768Hz output
4	IOD15	SD	IO	SD DATA2
5	IOD12	SD	IO	SD DATA3
6	IOD10	SD	IO	SD CMD
7	IOD11	SD	IO	SD CLK
8	IOD13	SD	IO	SD DATA0
9	IOD14	SD	IO	SD DATA1
10	IOA8	GPIO	IO	IOA8
11	IOA9	GPIO	IO	IOA9
12	IOA10	GPIO	IO	IOA10
13	IOA11	GPIO	IO	IOA11
14	IOA12	GPIO	IO	IOA12
15	IOA13	GPIO	IO	IOA13
16	IOA14	GPIO	IO	IOA14
17	IOA15	GPIO	IO	IOA15
18	VSS	Digital Ground	P	Digital ground
19	V33	IO PWR	P	3.3V IO power input
20	PLL_V33	PLL	P	3.3V PLL power input
21	X12MI_SINGLE	PLL	AI	X'tal 12MHz input
22	V12	CORE PWR	P	1.2V Core Power
23	PLL_VSS	PLL	P	PLL ground
24	IOB5	UART	IO	UART_TX
25	IOB4	UART	IO	UART_RX
26	IOB3	TFT	IO	TFT CLK
27	IOB2	TFT	IO	TFT VSYNC
28	IOB1	TFT	IO	TFT HSYNC
29	IOB0	TFT	IO	TFT DE
30	IOC12	ICE	IO	JTAG TDI
31	IOC13	ICE	IO	JTAG TDO
32	IOC14	ICE	IO	JTAG TCK/SWD SCK
33	IOC15	ICE	IO	JTAG TMS/SWD SWIO
34	IOB8	NAND	IO	NAND Flash Data bit 0
35	IOB9	NAND	IO	NAND Flash Data bit 1
36	IOB10	NAND	IO	NAND Flash Data bit 2
37	IOB11	NAND	IO	NAND Flash Data bit 3
38	IOB12	NAND	IO	NAND Flash Data bit 4
39	IOB13	NAND	IO	NAND Flash Data bit 5
40	IOB14	NAND	IO	NAND Flash Data bit 6
41	IOB15	NAND	IO	NAND Flash Data bit 7
42	USB_V33	USB	P	3.3V USB Power
43	DM	USB	AIO	USB DM
44	DP	USB	AIO	USB DP

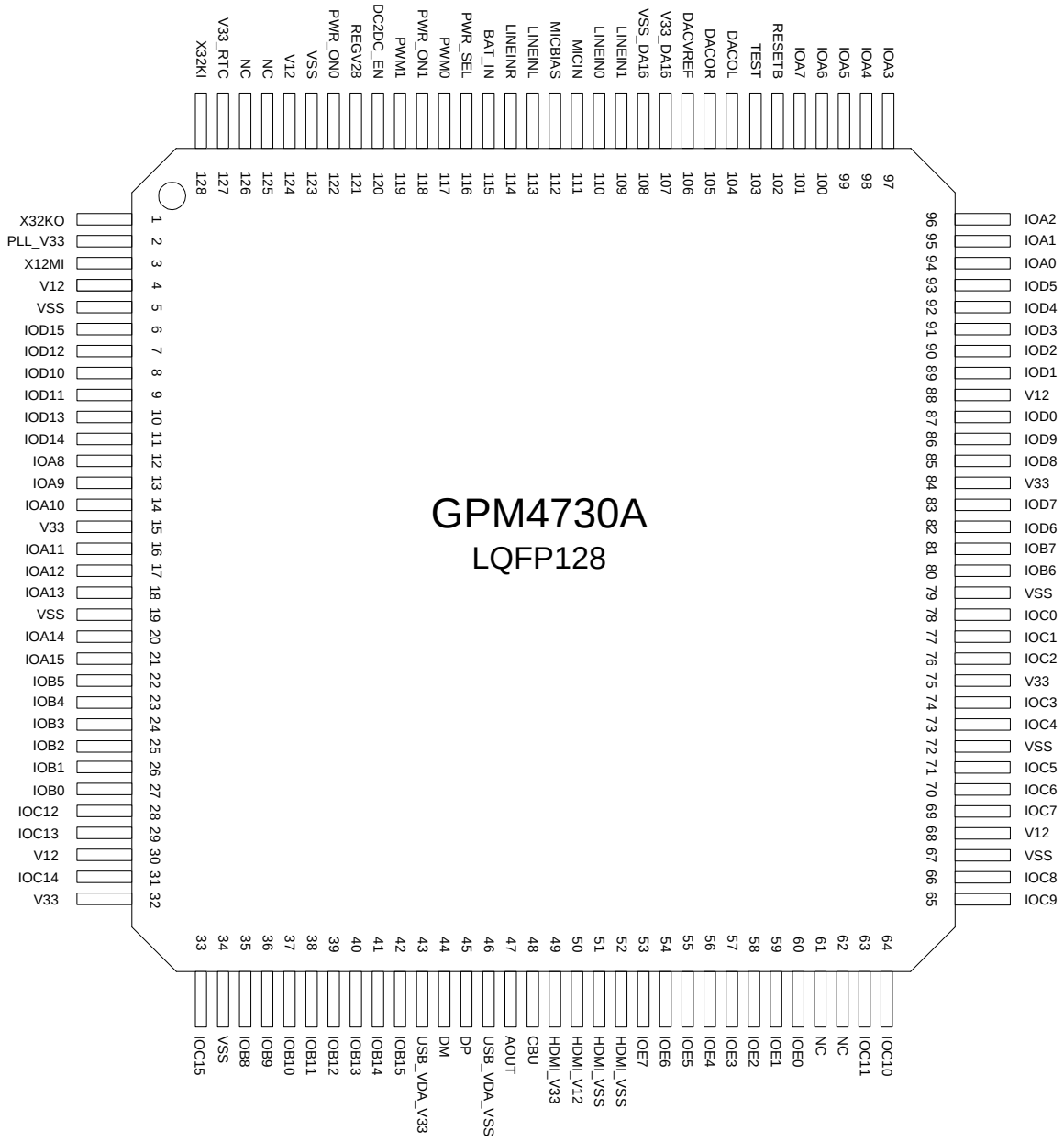
PKG No	Name	Group	Type	Normal Function Description
45	USB_VSS	USB	P	USB Ground
46	DDRVREF	DDR	P	DDR VREF 1.25V
47	DDRV25	DDR	P	DDR SSTL2 power input
48	DDRV25	DDR	P	DDR SSTL2 power input
49	V12	CORE PWR	P	1.2V Core Power input
50	DDRV25	DDR	P	DDR SSTL2 power input
51	DDRV25	DDR	P	DDR SSTL2 power input
52	DDRV25	DDR	P	DDR SSTL2 power input
53	DDRV25	DDR	P	DDR SSTL2 power input
54	HDMI_V33	HDMI	P	HDMI 3.3V power input
55	HDMI_V12	HDMI	P	HDMI 1.2V power input
56	HDMI_VSS	HDMI	P	HDMI ground
57	TXP2	HDMI	IO	HDMI TXP2/IOE7
58	TXN2	HDMI	IO	HDMI TXN2/IOE6
59	TXP1	HDMI	IO	HDMI TXP1/IOE5
60	TXN1	HDMI	IO	HDMI TXN1/IOE4
61	TXP0	HDMI	IO	HDMI TXP0/IOE3
62	TXN0	HDMI	IO	HDMI TXN0/IOE2
63	TXCP	HDMI	IO	HDMI TXCP/IOE1
64	TXCN	HDMI	IO	HDMI TXCN/IOE0
65	IOC11	MIPI	IO	MIPI0 CLKP/CSI VSYNC
66	IOC10	MIPI	IO	MIPI0 CLKN/CSI HSYNC
67	IOC9	MIPI	IO	MIPI0 DATA0P/CSI CLKO
68	IOC8	MIPI	IO	MIPI0 DATA0N/CSI CLKI
69	MIPI_V12	MIPI	P	MIPI 1.2V power input
70	IOC7	MIPI	IO	MIPI1 DATA0P/CSI D9
71	IOC6	MIPI	IO	MIPI1 DATA0N/CSI D8
72	IOC5	MIPI	IO	MIPI1 CLKP/CSI D7
73	IOC4	MIPI	IO	MIPI1 CLKN/CSI D6
74	IOC3	CSI	IO	CSI D5
75	V33	IO PWR	P	3.3V IO Power
76	IOC2	CSI	IO	CSI D4
77	IOC1	CSI	IO	CSI D3
78	IOC0	CSI	IO	CSI D2
79	VSS	Digital GND	P	Digital ground
80	IOB6	CSI	IO	CSI D0
81	IOB7	CSI	IO	CSI D1
82	IOD6	SPI	IO	SPI CS
83	IOD7	SPI	IO	SPI CLK
84	IOD8	SPI	IO	SPI TX
85	IOD9	SPI	IO	SPI RX
86	IOD0	SPIF	IO	SPI Flash CSB
87	IOD1	SPIF	IO	SPI Flash CLK
88	IOD2	SPIF	IO	SPI Flash RX0
89	IOD3	SPIF	IO	SPI Flash RX1

PKG No	Name	Group	Type	Normal Function Description
90	IOD4	SPIF	IO	SPI Flash RX2
91	IOD5	SPIF	IO	SPI Flash RX3
92	IOA0	TFT	IO	TFT D0
93	IOA1	TFT	IO	TFT D1
94	IOA2	TFT	IO	TFT D2
95	IOA3	TFT	IO	TFT D3
96	IOA4	TFT	IO	TFT D4
97	IOA5	TFT	IO	TFT D5
98	IOA6	TFT	IO	TFT D6
99	IOA7	TFT	IO	TFT D7
100	RESETB	SYSTEM	I	External RESETB(Low active)
101	TEST	SYSTEM	I	Test enable(High active)
102	VOL	AuDAC	AO	Audio DAC left channel output
103	VOR	AuDAC	AO	Audio DAC right channel output
104	VREF_DA16	AuDAC	AO	Audio DAC
105	V33_DA16	AuDAC	P	3.3V Power for AuDAC/CODEC ADC/SAR ADC
106	VSS_DA16	AuDAC	P	Ground for AuDAC/CODEC ADC/SAR ADC
107	V33_AD	SAR ADC	P	ADC 3.3V power input
108	VSS_AD	SAR ADC	P	ADC ground
109	LINEIN0_PAD	SAR ADC	AI	SAR ADC LINEIN0
110	LINEIN1_PAD	SAR ADC	AI	SAR ADC LINEIN1
111	LINEIN2_PAD	SAR ADC	AI	SAR ADC LINEIN2
112	VREF	CODEC_ADC	AO	CODEC ADC VREF
113	LINEINL	CODEC ADC	AI	CODEC ADC left channel input
114	MICIN	CODEC ADC	AI	CODEC ADC microphone input
115	LINEINR	CODEC ADC	AI	CODEC ADC right channel input
116	MICBIAS	CODEC ADC	AO	CODEC ADC microphone bias output
117	DDRV25	DDR	P	DDR SSTL2 power input
118	V12	CORE PWR	P	1.2V Core Power input
119	DDR_REG	SYSTEM	P	DDR LDO power output
120	REGV33	SYSTEM	P	LDO power input for DDR_REG/REGV28/REGV12
121	VSS	SYSTEM	P	Digital ground
122	REGV28	SYSTEM	P	LDO 2.8V power output
123	REGV12	SYSTEM	P	LDO 1.2V power output
124	PWR_ON0	SYSTEM	AI	Power on key input 0
125	PWR_ON1	SYSTEM	AI	Power on key input 1
126	PWR_ON2	SYSTEM	AI	Power on key input 2
127	PWR_ON3	SYSTEM	AI	Power on key input 3
128	DC2DC_EN	SYSTEM	AO	DC2DC enable output

Note: AO: Analog Output, AI: Analog Input

4.1. Package Pin Sequence

LQFP128 Package Top View



5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Rating

Rating	Symbol	Value	Unit
Supply Voltage 1	REGV33	-0.3 to 3.6	V
Supply Voltage 2	V33_RTC	-0.3 to 3.6	V
Supply Voltage 3	V33	-0.3 to 3.6	V
Supply Voltage 4	PLL_V33	-0.3 to 3.6	V
Supply Voltage 5	USB_V33	-0.3 to 3.6	V
Supply Voltage 6	HDMI_V33	-0.3 to 3.6	V
Supply Voltage 7	V33_DA16	-0.3 to 3.6	V
Supply Voltage 8	V33_AD	-0.3 to 3.6	V
Supply Voltage 9	REG28	-0.3 to 3.6	V
Supply Voltage 10	DDRV25	-0.3 to 3.6	V
Supply Voltage 11	DDR_REG	-0.3 to 3.6	V
Supply Voltage 12	HDMI_V12	-0.3 to 1.4	V
Supply Voltage 13	MIPI_V12	-0.3 to 1.4	V
Supply Voltage 14	V12	-0.3 to 1.4	V
Input Voltage	V_{IN}	-0.3 to 3.6	V
Operating Temperature	T_A	-40~70	℃
Storage Temperature	T_{STG}	-40 to +150	℃

5.2. DC Characteristics

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Supply Voltage 1	REGV33	2.7	3.3	3.6	V	-
Supply Voltage 2	V33_RTC	2.7	3.3	3.6	V	-
Supply Voltage 3	V33	2.7	3.3	3.6	V	-
Supply Voltage 4	PLL_V33	2.7	3.3	3.6	V	-
Supply Voltage 5	USB_V33	3.0	3.3	3.6	V	-
Supply Voltage 6	HDMI_V33	2.7	3.3	3.6	V	-
Supply Voltage 7	V33_DA16	2.7	3.3	3.6	V	-
Supply Voltage 8	V33_AD	2.7	3.3	3.6	V	-
Supply Voltage 9	REG28	2.43	2.8	3.41	V	-
Supply Voltage 10	DDRV25	2.25	2.5	2.75	V	-
Supply Voltage 11	DDR_REG	2.25	2.5	2.75	V	-
Supply Voltage 12	HDMI_V12	1.2	1.32	1.4	V	-
Supply Voltage 13	MIPI_V12	1.2	1.32	1.4	V	-
Supply Voltage 14	V12	1.2	1.32	1.4	V	-
Operating Current Case 1	I_{OP1}	-	280	-	mA	Core power current@193.5MHz, V33=3.3V, V12=1.32V , Sensor(MIPI) + ISP + H.264 encode +TFT working + all clocks turn on
Operating Current Case 2	I_{OP2}	-	245	-	mA	Core power current@144MHz, V33=3.3V, V12=1.32V , Sensor(MIPI) + ISP + H.264

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
						encode +TFT working + all clocks turn on
Operating Current Case 3	I_{OP3}	-	190	-	mA	Core power current@144MHz, V33=3.3V, V12=1.32V , PPU + TFT working + all clocks turn on
Sleep Current	I_{SLEEP}	-	3	-	mA	REGV33=3.3V, V33=3.3V,V12=1.2V All clock and all macro are turn off.
Power Down Current	I_{PD}	-	20	-	μA	All power is off except RTC macro (RTC_V33=3.3V, the others=0V)
High Input Voltage	V_{IH}	0.7V33	-	V33	V	-
Low Input Voltage	V_{IL}	VSS	-	0.3V33	V	-
Crystal Frequency 1	-	-	32768	-	Hz	-
Crystal Frequency 2	$F_{CRYSTAL}$	-	12	-	MHz	-
System Clock	F_{SYS}	256Hz[1]	-	144	MHz	-

Note1: By setting clock divider and changing system clock to SLOW mode (32768Hz).

5.3. Audio DAC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	-	-	16	Bit	-
Full Scale Output Voltage	-	0.6*V33_DA16	-	Vp-p	-
THD+N (Fin = 0.997kHz)	-	0.1	-	%	-
Dynamic Range	71	74	-	dB	Fin=0.997KHz w/ -60dB output loading=32 ohm
Output Loading	32	-	-	ohm	-
Frequency Response	20	-	19200	Hz	-

5.4. CODEC ADC/MIC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	-	-	16	Bit	-
Input Voltage Range	2.7	-	3.6	V	-
SNR	-	85	-	dB	Boost=0dB, PGA=0dB, filter: 20K LPF + A weighting@V33_DA16=3.3V
THD+N	-	78	-	dB	Boost=0dB, PGA=0dB, Fin=0.997KHz, Fs=48kHz @V33_DA16=3.3V
Dynamic Range	-	84.7	-	dB	Boost=0dB, PGA=0dB, filter: 20K LPF + A weighting

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
					@V33_DA16=3.3V
MICBIAS	-	2.45	-	V	-
VREF	-	1.65	-	V	-

5.5. SAR ADC Characteristics

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SAR ADC Input Voltage Range	VIN_RANGE	2.7	-	3.6	V
Resolution of ADC	RESO	-	12	-	bit
Signal-to-Noise Plus Distortion of ADC from Line in	SINAD (Note 1)	-	59.88	-	dB
Effective Number of Bit	ENOB (Note 2)	-	9.66	-	bit
Integral Non-Linearity of ADC	INL	-	7	-	LSB (Note 4)
Differential Non-Linearity of ADC	DNL (Note 3)	-	6	-	LSB
No Missing Code		-	10	-	bit
AD Conversion Rate=ADCCLK/16	F_{CONV}	-	-	125K	Hz

Note1: The SINAD testing condition at VINLp-p = 0.8 * V33_AD, F_{CONV} = 62.5KHz, Fin = 1.0KHz Sine waves at V33_AD = 3.0V from ADC input.

Note2: ENOB = (SINAD - 1.76) / 6.02.

Note3: This ADC guarantees no missing code at 10-bit resolution.

Note4: LSB means Least Significant Bit (at 12-bit resolution).

5.6. DDR Regulator for DDR Characteristics

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.7	-	3.6	V
Maximum Current Output	IREGO	-	-	150	mA
Output Voltage	VREGO	2.25	2.5	2.75	V
Standby Current	IREGS	-	-	2	uA

5.7. 3.3V-to-1.2V Regulator for Core Characteristics

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.7	-	3.3	V
Maximum Current Output	IREGO	-	-	350	mA
Output Voltage	VREGO	1.08	1.2	1.32	V
Standby Current	IREGS	-	-	2	uA

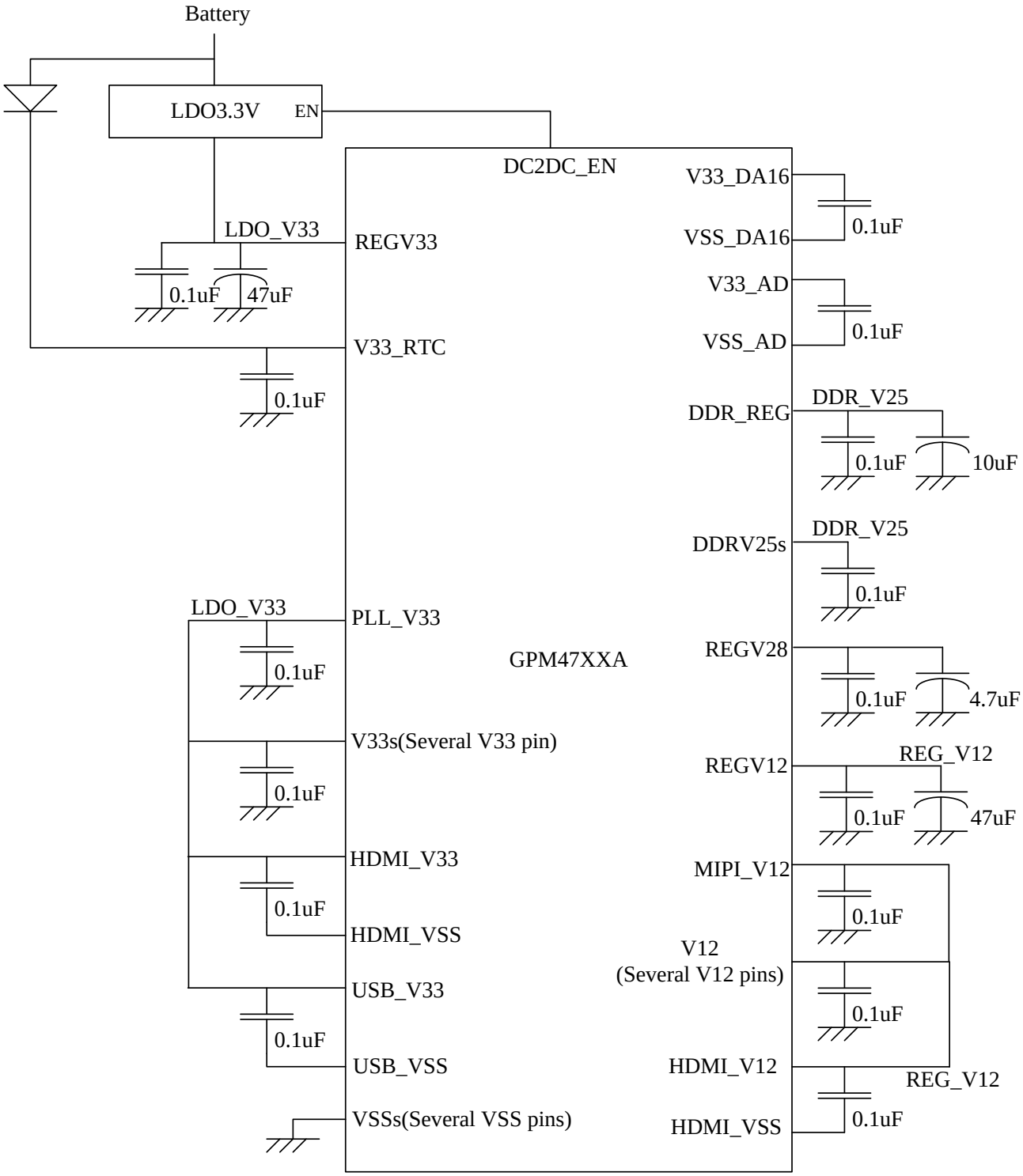
5.8. 3.6V-to-2.8V Regulator for Sensor Characteristics

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	3.0	-	3.6	V
Maximum Current Output	IREGO	-	-	60	mA
Output Voltage	VREGO	2.8	3.3	3.3	V
Standby Current	IREGS	-	-	2	uA

6. RECOMMENDED BOARD LAYOUT

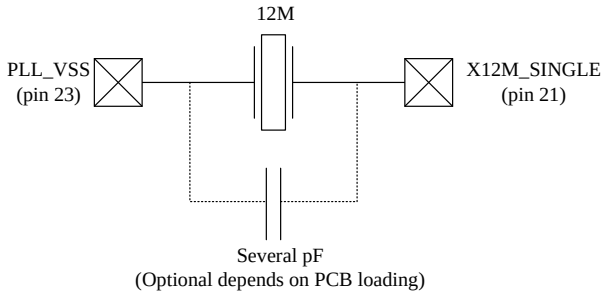
6.1. Power and Ground

All power and ground pins are connected as in the following diagram for general application. The decoupling capacitor of 0.1μF, 10μF, and 47uF should be connected to each corresponding power pin of IC and 0.1uF capacitor must be as close as possible to the power pin. Each V33/V12 requires one 0.1μF capacitor and must be as close as possible to the power pin.

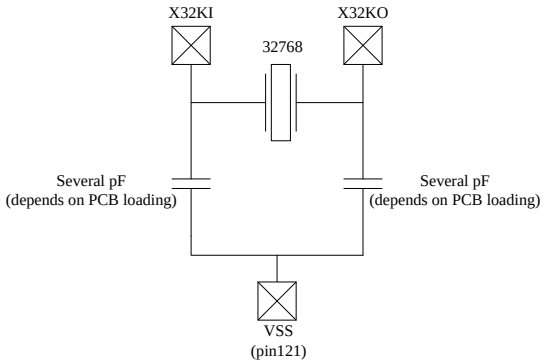


6.2. Crystal and PLL

When the 12MHz crystal is applied in the system, please connect the crystal circuit as indicated in the following diagram.



Note*: Please refer to the crystal's application circuit.



A Crystal (32768Hz) may be used for applications that may involve with precise time clock requirement. See the above diagram for more details.

Note*: Please refer to the crystal's application circuit.

7. PACKAGE/PAD LOCATIONS

7.1. Ordering Information

Product Number	Package Type
GPM4730A-NnnV-QL09x	Halogen Free Package

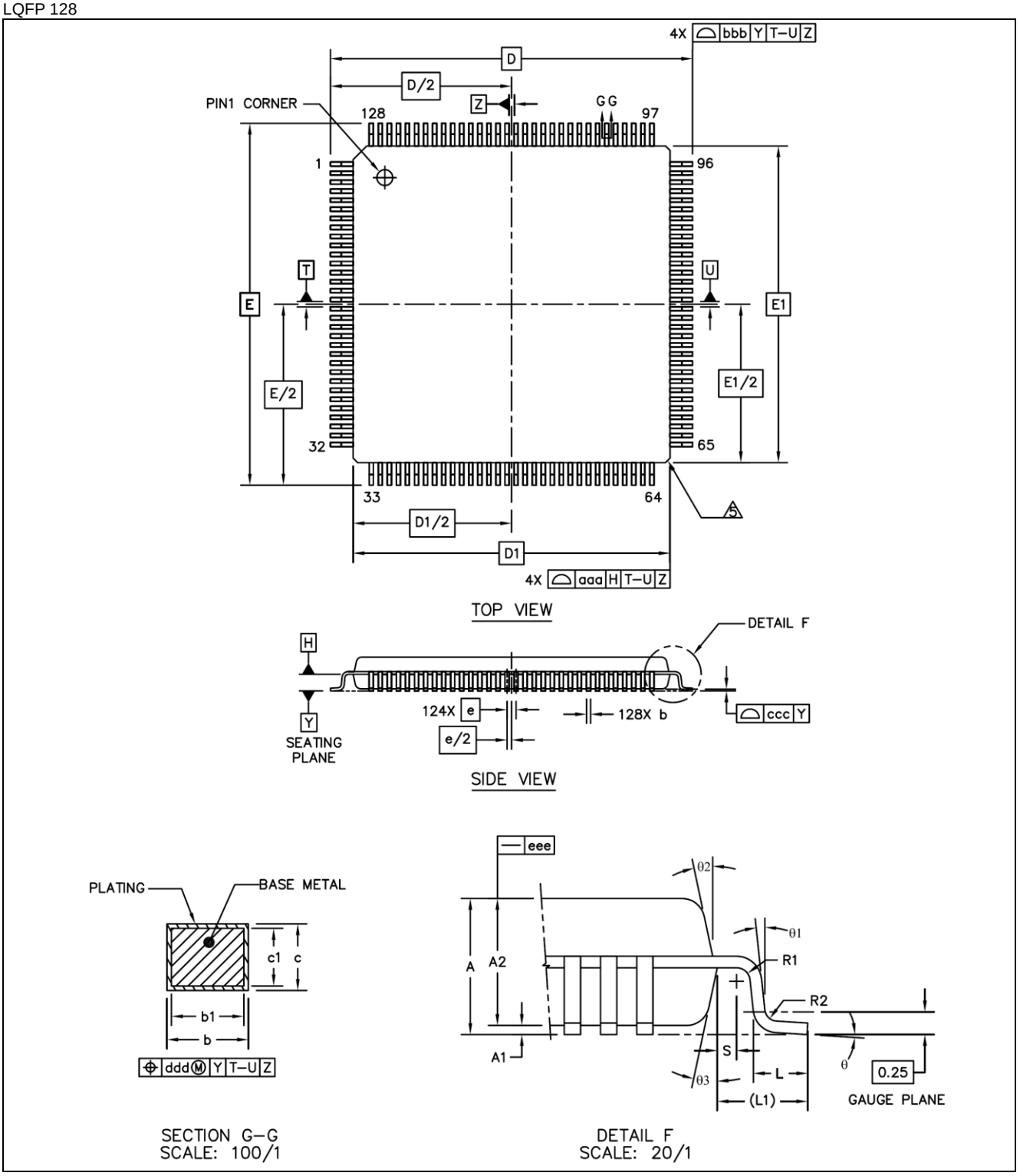
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

7.2. Package Information

LQFP 128



Symbol	Millimeter		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45

Symbol	Millimeter		
	Min.	Nom.	Max.
b	0.13	0.16	0.23
b1	0.13	-	0.19
c	0.09	-	0.20
c1	0.09	-	0.16
D	16.00 BSC		
E	16.00 BSC		
D1	14.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°
θ1	0°	-	-°
θ2	11°	12°	13°
θ3	11°	12°	13°
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
aaa	0.10		
bbb	0.20		
ccc	0.08		
ddd	0.07		
eee	0.05		

8. DISCLAIMER

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9. REVISION HISTORY

Date	Revision #	Description	Page
Mar. 03, 2016	0.1	Preliminary version.	18