DATA SHEET

GPC74C Series

4-bit Speech with SPU

Sep. 02, 2020

Version 1.3

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Table of Contents

PAGE

1 GPC74C SERIES: 3
2 GENERAL DESCRIPTION 3
3 BLOCK DIAGRAM 3
4 FEATURES 3
5 APPLICATION FIELD 3
6 SIGNAL DESCRIPTIONS 4
6.1 PACKAGE PAD ASSIGNMENT 5
6.1.1 Package for GPC74C340B/GPC74P170B/GPC74C080B/GPC74P064B/GPC74P048B 5
6.1.2 Package for GPC74C032B/GPC74C016B 6
7 FUNCTION DESCRIPTIONS 7
7.1 CPU 7
7.2 MEMORY 7
7.3 CLOCK SOURCE 7
7.4 LOW VOLTAGE RESET 7
7.5 INTERRUPT 7
7.6 SPU 7
7.7 PWM 7
7.8 SLEEP MODE, WAKEUP AND WATCHDOG 7
7.9 I/O 7
8 ELECTRICAL SPECIFICATIONS 8
8.1 DC CHARACTERISTICS (VDD = 3/4.5V (IOA ~ IOD), TA = 25℃) 8
8.2 INTERNAL FREQUENCY (FOSC) AND VDD 9
8.3 INTERNAL FREQUENCY (FOSC) AND TEMPERATURE 9
8.4 OPERATING CURRENT(IOP) AND VDD 10
9 APPLICATION CIRCUITS 11
9.1 LIGHT LOADING AND CIRCUIT WITHOUT NOISE 11
9.2 HEAVY LOADING OR CIRCUIT WITH NOISE 12
9.3 CURRENT DAC APPLICATION CIRCUIT 13
10 PACKAGE/PAD LOCATIONS 14
10.1 ORDERING INFORMATION 14
10.2 PACKAGE INFORMATION 15
11 DISCLAIMER 18
12 REVISION HISTORY 19

4-BIT SPEECH WITH SPU

1 GPC74C SERIES:

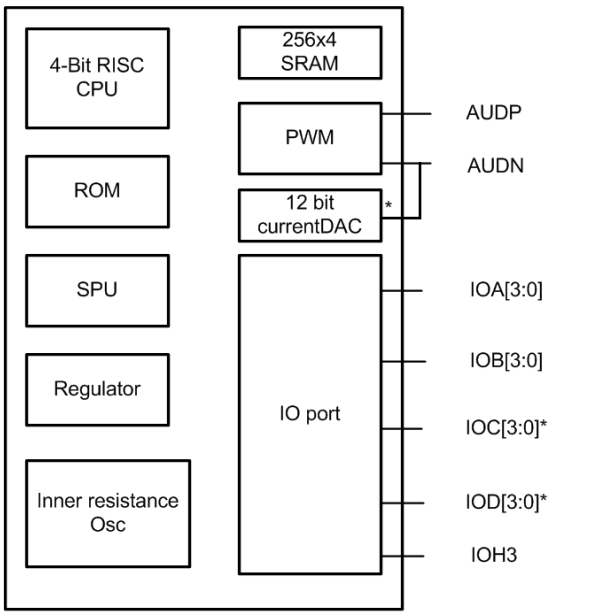
Product No.	GPC74C016B	GPC74C032B	GPC74C048B	GPC74C064B	GPC74C080B	GPC74C170B	GPC74C340B
ROM Density	32K X 12	64K X 12	96K X 12	128K X 12	160K X 12	340K X 12	680K X 12
IOs	9	9	17	17	17	17	17
Current DAC embedded	No	No	Yes	Yes	Yes	Yes	Yes

Note: 9 IOs are IOA[3:0], IOB[3:0] and IOH3, 17 IOs are IOA[3:0], IOB[3:0], IOC[3:0], IOD[3:0], IOH3;IOA/IOB/IOC/IOD can be configured as input or output pin;IOH3 is **input only** pin with pull low resistor

2 GENERAL DESCRIPTION

GPC74C, a 4-bit sound controller, is architected with a four-channel SPU for MIDI playback, a 4-bit RISC CPU, a 14-bit PWM, 8/16 IOs and 1 input pin (with pull low resistor) , 256-nibble RAM, and embedded ROM with density of 32K/ 64K/ 96K/ 128K/ 160K/ 340K/ 680K x 12-bit of memory space. The operating voltage ranges from 2.0V through 5.5V and operating speed is 1M/2MHz, configurable through inner oscillator. Other features include Low Voltage Reset, IR carry output, Watchdog, five interrupt sources with two time-bases, etc.

3 BLOCK DIAGRAM



* Not available in GPC74C016B/GPC74C032B

4 FEATURES

- 4-bit RISC CPU
- CPU Clock: 1M/2M Hz, System clock: 8MHz
- Operating Voltage: 2.0V - 5.5V
- Regulator built-in with input voltage: 2.0~5.5V, output voltage: 2.0~3.0V
- IO: IOA~IOD, IOH3 Operating Voltage: 2.0V - 5.5V
- 256 nibbles SRAM
- 14-bit PWM driver for driving speaker directly
- 12-bit Current DAC embedded, except GPC74C032B/ GPC74C016B
- 32K/64K/96K/128K/160K/340K/680K x12-bit ROM for different body
- Standby mode for power savings
- Five interrupt sources with two Time-bases
- 4-channel Sound Processing Unit (SPU) supporting MIDI playback
- 8/16 general IOs (bit programmable), one input pin with pull low resistor
- Key wakeup function
- Low voltage reset
- Watchdog
- Low Voltage Detection

7-level (2.2V/ 2.4V/ 2.6V/ 2.8V/ 3.0V/ 3.3/ 3.6V) voltage detector

5 APPLICATION FIELD

- Talking instrument controller
- General Music Synthesizer
- Toy controller
- Intelligent toy controller
- And more

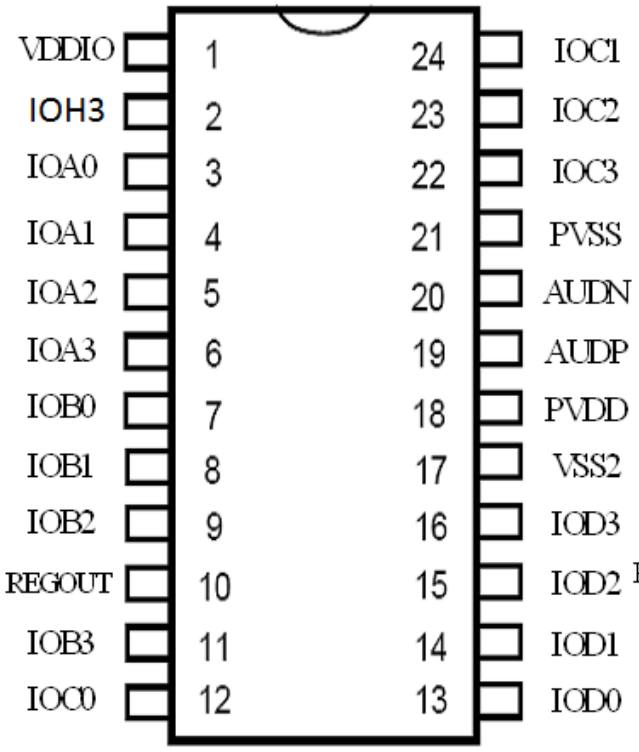
6 SIGNAL DESCRIPTIONS

PIN Name	Type	Description
IOA[3：0]	I/O	IOA[3：0] is a bi-directional I/O port with wakeup capability (via body option). 1Mohm || 200K feedback Pull Low resistor IOA2 shares pad with External Interrupt Input (via body option) IOA1 shares pad with IR Output (via body option) IOA0 shares pad with Key Reset Input (via body option)
IOB[3：0]	I/O	IOB[3：0] is a bi-directional I/O port with wakeup capability (via body option). 1Mohm || 200K feedback Pull Low resistor IOB2 shares pad with External Interrupt Input (via body option) IOB1 shares pad with IR Output (via body option) IOB0 shares pad with Key Reset Input (via body option)
IOC[3：0]	I/O	Not available for GPC74C032B/GPC74C016B IOC[3：0] is a bi-directional I/O port with wakeup capability (via body option). 1Mohm || 200K feedback Pull Low resistor IOC2 shares pad with External Interrupt Input (via body option) IOC1 shares pad with IR Output (via body option) IOC0 shares pad with Key Reset Input (via body option)
IOD[3：0]	I/O	Not available for GPC74C032B/GPC74C016B IOD[3：0] is a bi-directional I/O port with wakeup capability (via body option). 1Mohm || 200K feedback Pull Low resistor IOD2 shares pad with External Interrupt Input (via body option) IOD1 shares pad with IR Output (via body option) IOD0 shares pad with Key Reset Input (via body option)
AUDP	O	PWM audio output and it will be a floating pad in Current DAC mode
AUDN	O	PWM audio output and it will be an audio output in Current DAC mode
VDDIO	P	Power supply voltage input
VSS	G	Ground reference
IOH3	I	IOH3 : input port with pull low resistor & wakeup capability (body option)
REGOUT	P	3.3V regulator output for core power
PVDD	P	PWM driver power
PVSS	G	PWM driver ground reference

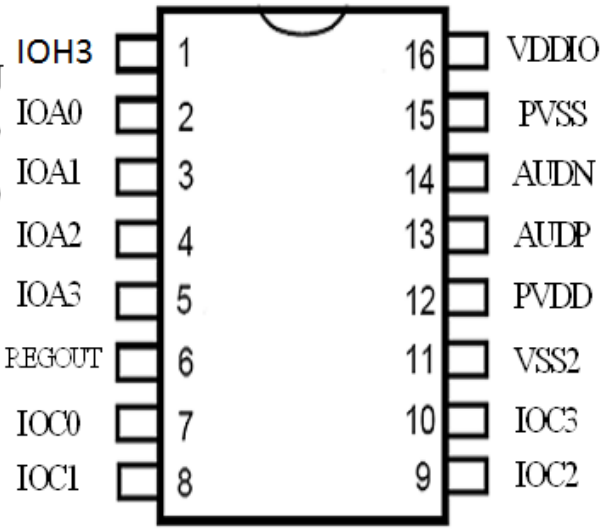
6.1 Package Pad Assignment

6.1.1 Package for GPC74C340B/GPC74P170B/GPC74C080B/GPC74P064B/GPC74P048B

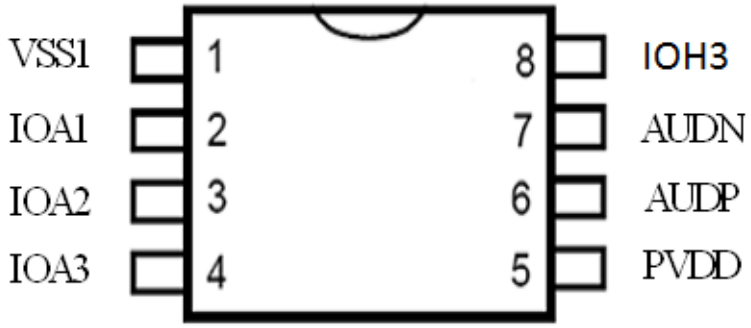
24 PIN SOP（300 mil）



16 PIN SOP（150 mil）

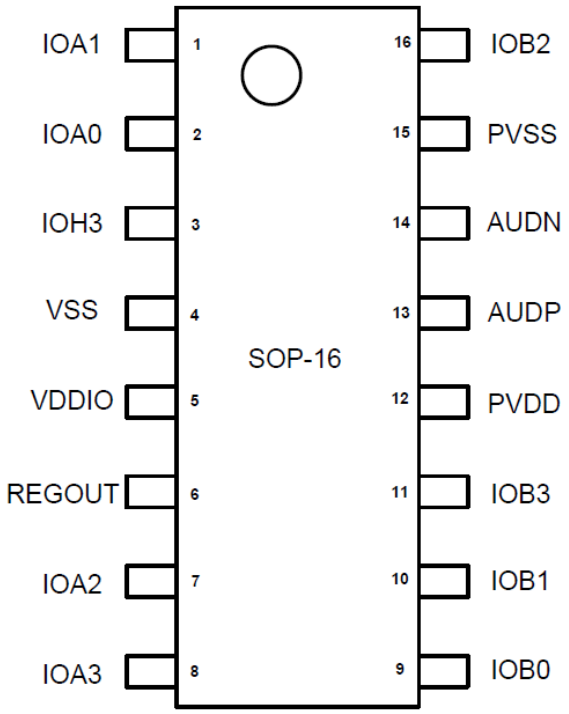


8 PIN SOP（150 mil）

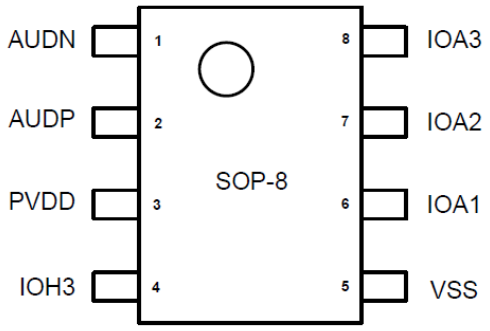


6.1.2 Package for GPC74C032B/GPC74C016B

16-PIN SOP（150 mil）



8-PIN SOP（150 mil）



7 FUNCTION DESCRIPTIONS

7.1 CPU

GPC74C features a 4-bit RISC CPU, executing the 12-bit instruction set with total of 72 instructions available, 7 stacks managed by 3-bit stack pointer, three DPRs(Data Pointer to read ROM) sharing stack 4 ~ 6, and 8 VPRs(Voice Data Pointer) for SPU.

7.2 Memory

7.2.1 SRAM

There are 256 nibbles of SRAM, grouped into four banks. Each bank has 64 nibbles and supports index mode to read/write its content addressed by TXR.

7.2.2 ROM

GPC74C provides 32K/64K/96K/128K/160K/340K/680K X12-bit ROM for different body.

7.3 Clock Source

Clock source is an inner resistant oscillator with CPU clock options of 1MHz or 2MHz

7.4 Low Voltage Reset

With the LVR function, a reset signal is generated to reset system when the operating voltage drops below LVR level.

7.5 Interrupt

An interrupt is a special event request to microcontroller. When it occurs, the corresponding interrupt will activate and direct the program code to execute the respective functions. GPC74C has five interrupt sources. Please refer to programming guide for more details.

7.5.1 Timebase

There are two Time-base, TB1/TB2, generated by system clock. The interval of TB1 is allowed up to 1ms and TB2 is up to 2ms.

7.6 SPU

Four-channel SPU supports MIDI playback with A3400Pro-like decode or PCM format and each channel has an 8-bit envelop control.

7.7 PWM

The PWM module is a 14-bit PWM driver to drive speaker directly.

7.8 Sleep Mode, Wakeup and Watchdog

7.8.1 Sleep mode and wakeup

Sleep mode or known as power down mode is an operating state that requires an extremely low power consumption to maintain the system in active. The sleep mode is particularly useful for the application areas where the system is required to constantly maintain its basic functionality and where the power capacity is limited. GPC74C will enter sleep mode when SLEEP instruction is executed and can be waked up by interrupt or key change. CPU will continue to execute the program from where it entered sleep mode.

7.8.2 Watchdog Reset

A watchdog reset is a reset signal that is generated to reset the entire system when watchdog counter is overflow. In case when the program code has been running into an unknown state and without the watchdog signal being cleared for a certain period of time, watchdog function automatically generates a reset signal pulling the system back from unknown state.

7.9 I/O

GPC74C features 8/16-bit programmable IOs with wakeup capability and 1 bit input port with pull low resistor & wakeup capability. These IOs normally support input with floating or pull-low and output options. In addition to the ordinary IO function, some IO ports have special functions. The following table summarizes the special functions for these IOs.

Special Function in Port

Port	Special Function	Function Description	Note
IOA0/IOB0	Key Reset	Key reset pin selected by code option	
IOA1/IOB1	IROUT	IR carry output selected by code option	
IOA2/IOB2	EXT INT	External interrupt input selected by code option	

8 ELECTRICAL SPECIFICATIONS

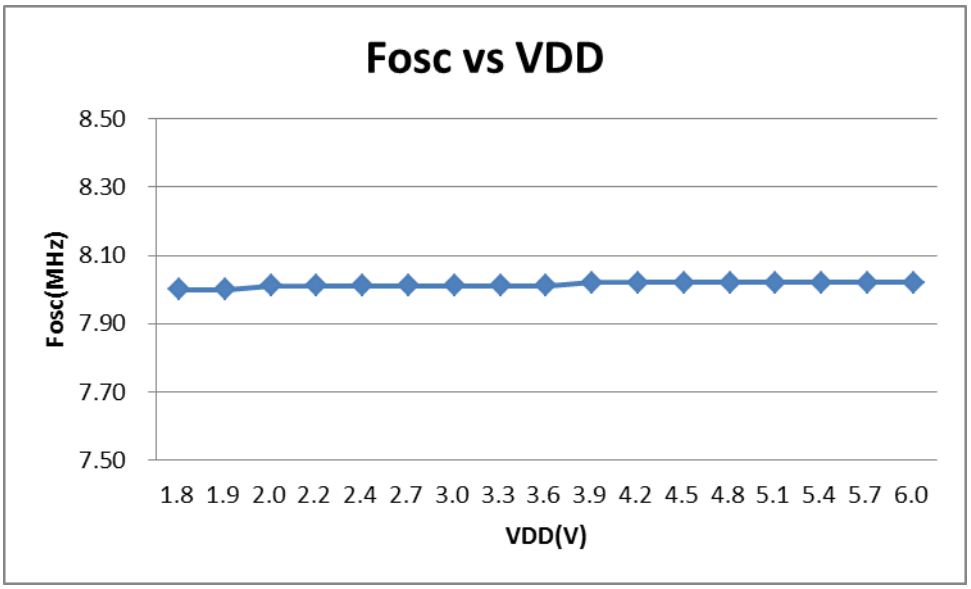
Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	(VSS-0.3V) to (V_+ + 0.3V)
Operating Temperature	T_A	0℃ to +70℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions, see DC Electrical Characteristics.

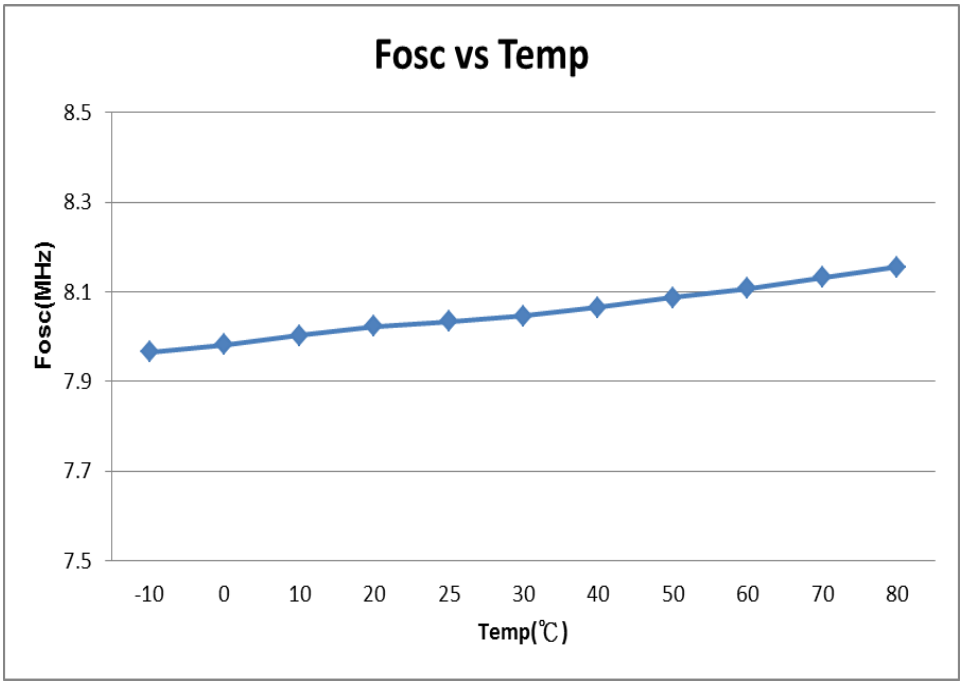
8.1 DC Characteristics (VDD = 3/4.5V (IOA ~ IOD), TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.0	-	5.5	V	
Operating Current	I_{OP}	-	1.5	2.6	mA	F_{CPU} = 2MHz @ 3.0V, PWM output off
		-	2	5.2	mA	F_{CPU} = 2MHz @ 4.5V, PWM output off
Standby Current	I_{STBY}	-	-	5	uA	VDD = 3.0V
		-	-	5	uA	VDD = 4.5V
GPIO Input High Level (IOA, IOB, IOC, IOD)	V_{IH}	0.5VDD	-	-	V	VDD = 4.5V
GPIO Input Low Level (IOA, IOB, IOC, IOD)	V_{IL}	-	-	0.5VDD	V	VDD = 4.5V
Output High Current (IOA, IOB, IOC, IOD)	I_{OH}	7	10	13	mA	VDD = 3.0V, V_{OH} = 0.7*VDD
		14	20	26	mA	VDD = 4.5V, V_{OH} = 0.7*VDD
Output Low Current (Normal)	I_{OL1}	7	10	13	mA	VDD = 3.0V, V_{OL} = 0.3*VDD
		14	20	26	mA	VDD = 4.5V, V_{OL} = 0.3*VDD
Output Low Current (High sink , by Body Option)	I_{OL2}	10	20	30	mA	VDD = 3.0V, V_{OL} = 0.3*VDD
		20	40	60	mA	VDD =4.5V, V_{OL} = 0.3*VDD
Input Pull Low Resistor (IOA, IOB, IOC, IOD)	R_{L1}	140	200	260	Kohm	VDD = 3.0V, IO = 0V
		70	100	130	Kohm	VDD = 4.5V, IO = 0V
Input Pull Low Resistor (IOA, IOB, IOC, IOD)	R_{L2}	700	1000	1300	Kohm	VDD = 3.0V, IO = 3.0V
		350	500	650	Kohm	VDD = 4.5V, IO = 4.5V
PWM Driver Current	I_{PWM}	126	180	234	mA	VDD = 3.0V, 8 Ohms load
		196	280	364	mA	VDD = 4.5V, 8 Ohms load
Frequency deviation by voltage drop	△F/F	-1	-	+1	%	$\frac{Fosc(5.5v) - Fosc(2.4v)}{Fosc(3.0v)}$ F_{CPU} = 2MHz
Frequency lot deviation	△F/F	-1	-	1	%	$\frac{Fmax(3.0v) - Fmin(3.0v)}{Fmax(3.0v)}$ F_{CPU} = 2MHz @ 3.0V (tentative)
		-1	-	1	%	$\frac{Fmax(4.5v) - Fmin(4.5v)}{Fmax(4.5v)}$ F_{CPU} = 2MHz @ 4.5V (tentative)

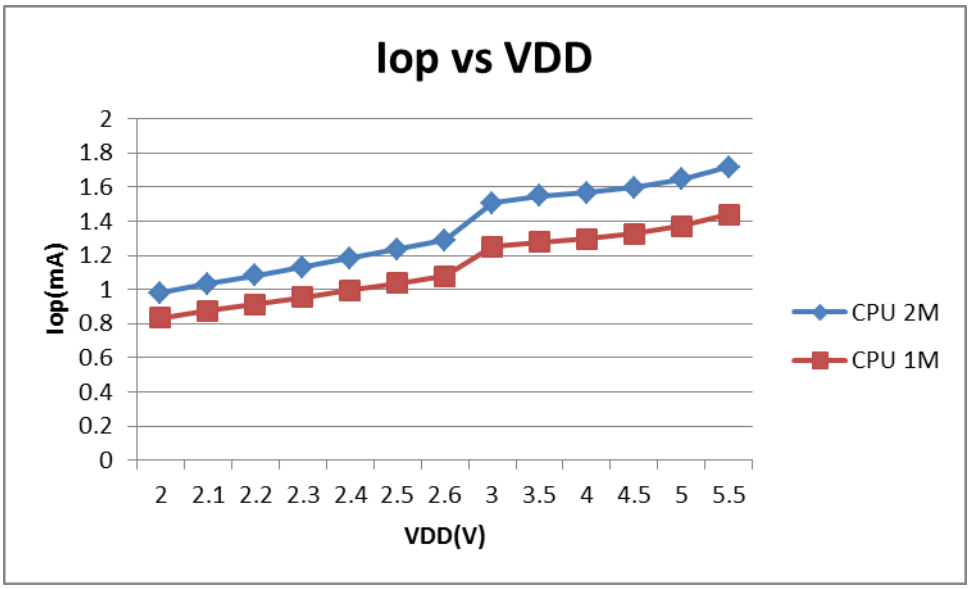
8.2 Internal Frequency (Fosc) and VDD



8.3 Internal Frequency (Fosc) and Temperature

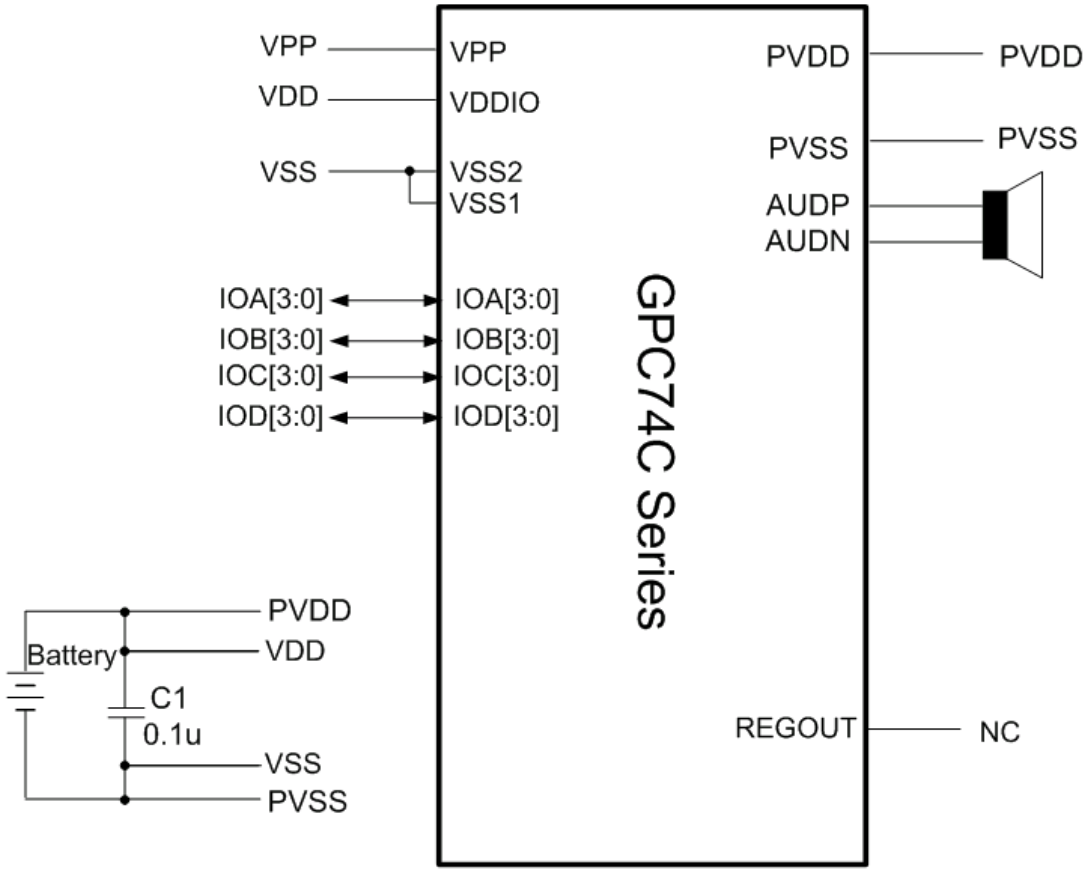


8.4 Operating Current(Iop) and VDD



9 APPLICATION CIRCUITS

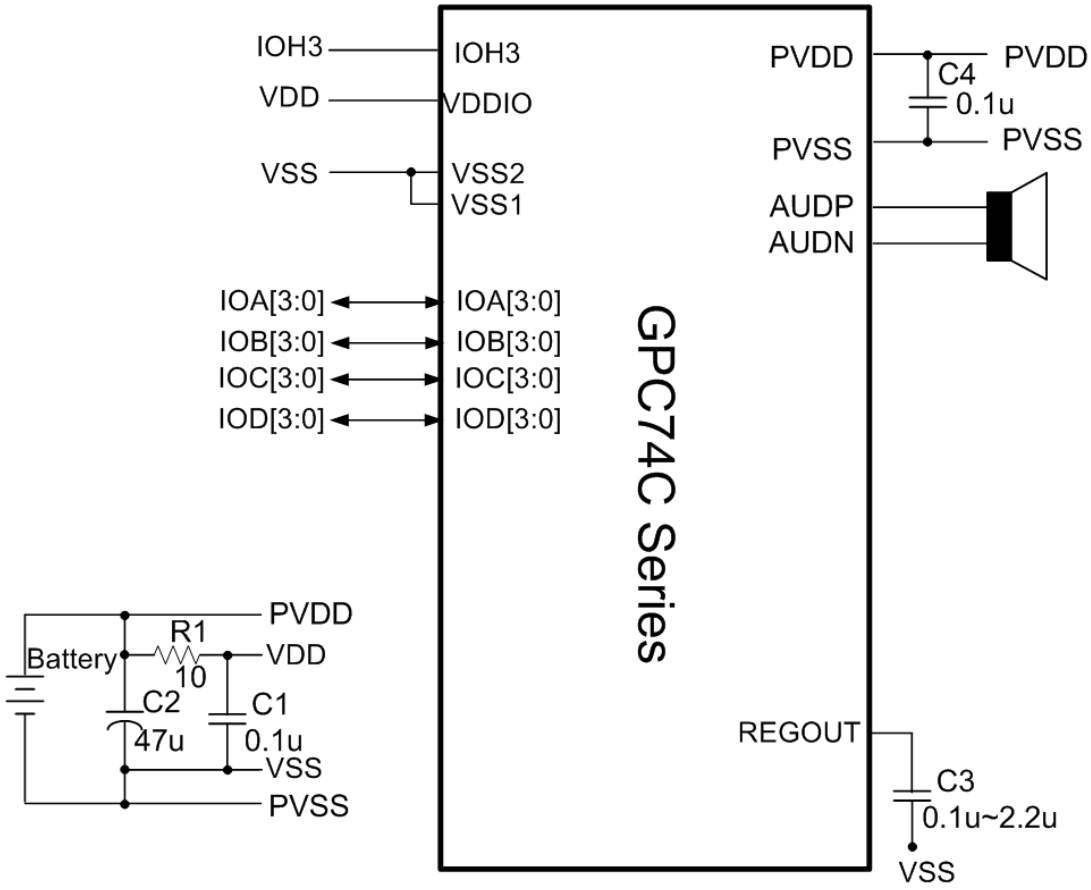
9.1 Light Loading and Circuit without Noise



PCB Layout Guidelines:

1. PVDD can be higher than or equal to VDD.
2. VSS, PVSS must be connected to ground input directly, not the branch of each other.
3. When using two batteries, 0.1uF ~ 4.7uF is suggested for C1 and it should be increased in a high volume application.

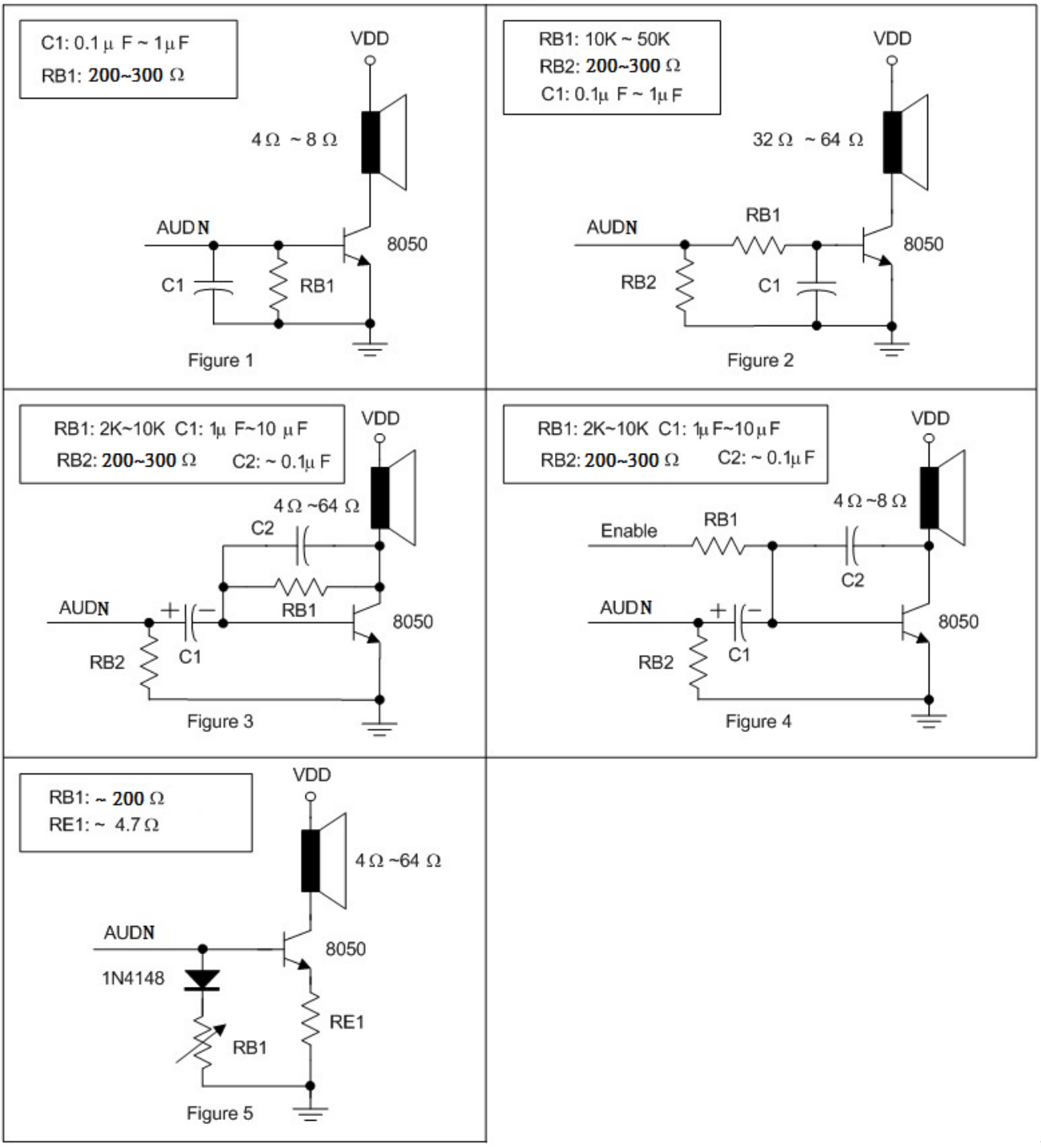
9.2 Heavy Loading or Circuit with Noise



PCB Layout Guidelines:

1. PVDD can be higher than or equal to VDD.
2. VSS, PVSS must be connected to ground input directly, not the branch of each other.
3. A typical value of C2 is 47uf, and it should vary in different loadings.
4. If there is application with motor, REGOUT should be connected with C4.

9.3 Current DAC Application Circuit



10 PACKAGE/PAD LOCATIONS

10.1 Ordering Information

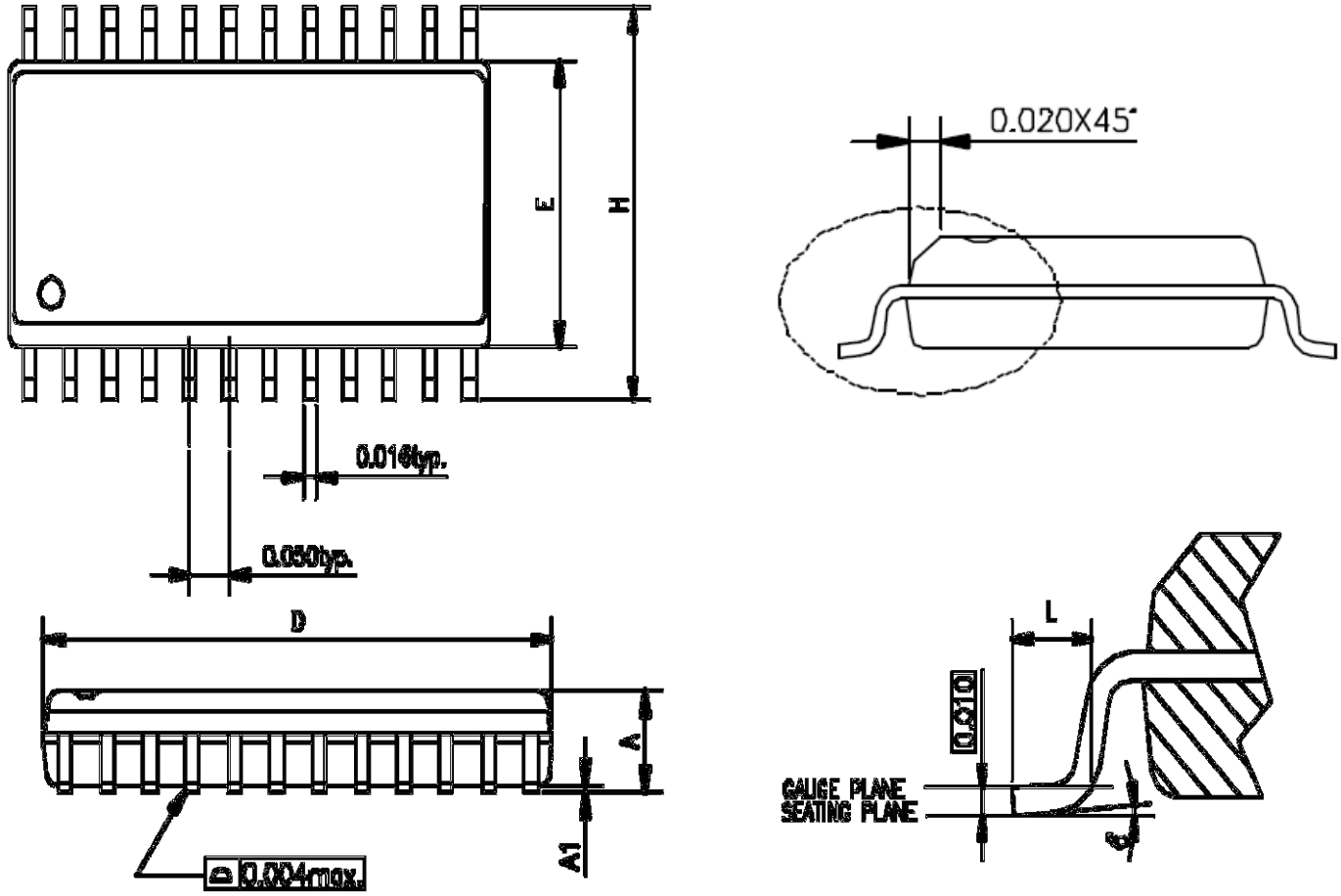
Product Number	Package Type
GPC74CXXXB-NnnV-C	Chip form
GPC74CXXXB-HS01X	Green Package –SOP8
GPC74CXXXB-HS03X	Green Package –SOP16
GPC74CXXXB-HS10X	Green Package –SOP24

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10.2 Package Information

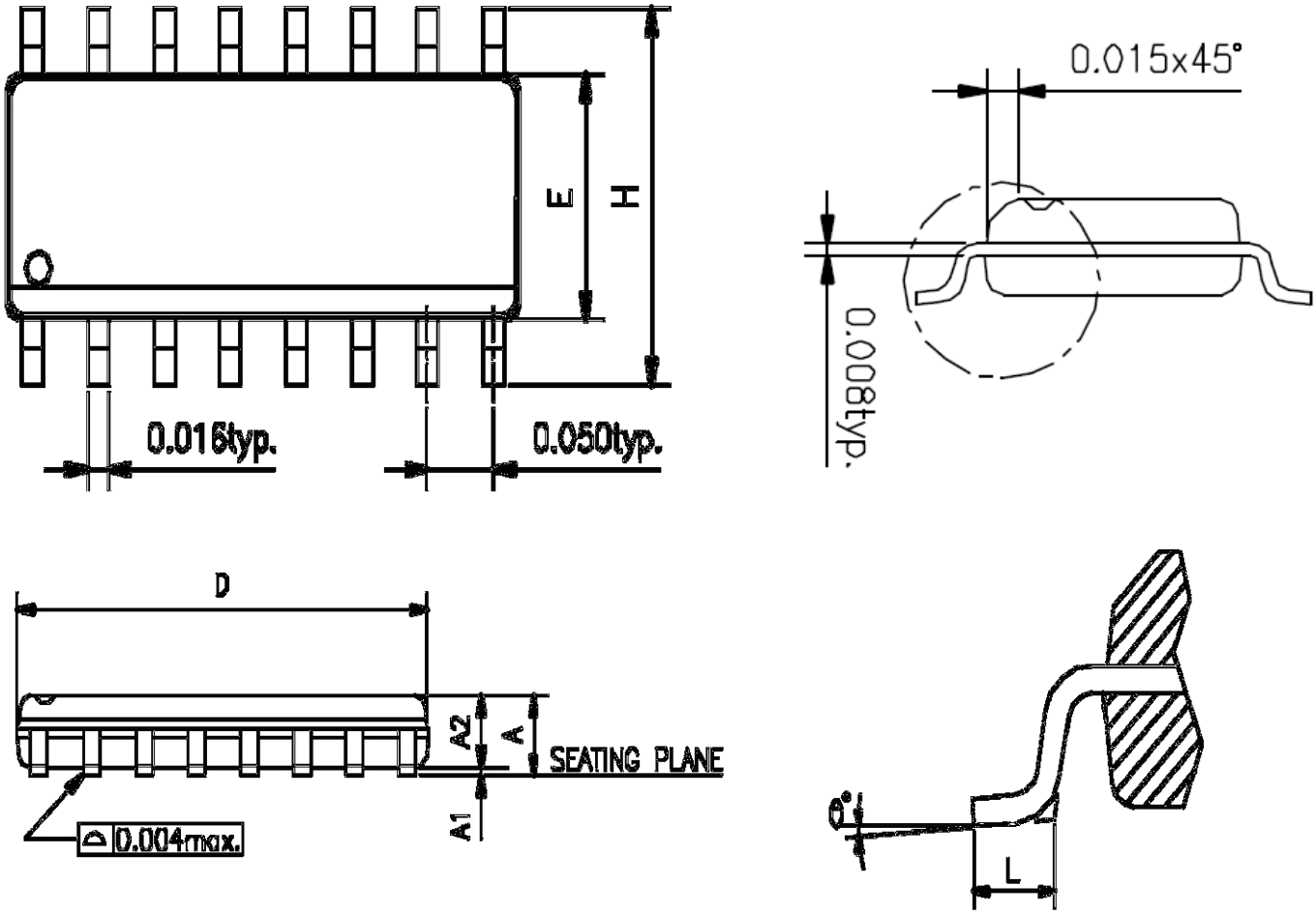
24 PIN SOP(300 mil)



SYMBOLS	MIN.	NOM	MAX.
A	0.093	0.099	0.104
A1	0.004	—	0.012
D	0.599	0.600	0.614
E	0.291	0.295	0.299
H	0.394	0.406	0.419
L	0.016	0.035	0.050
θ°	0	—	8

UNIT : INCH

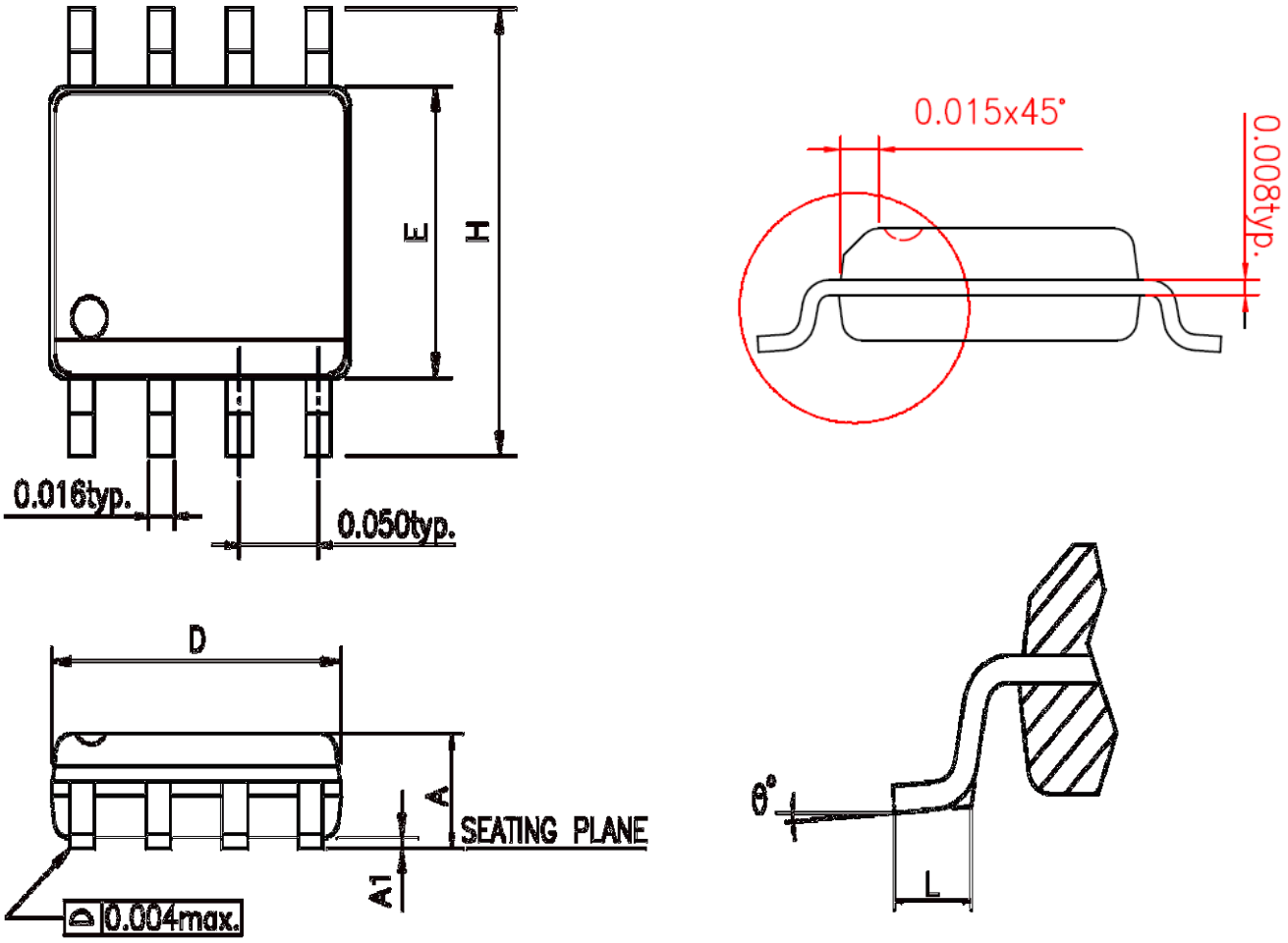
16 PIN SOP(150 mil)



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

8 PIN SOP(150 mil)



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

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12 REVISION HISTORY

Date	Revision #	Description	Page
Sep. 02, 2020	1.3	Update current DAC application circuit	13
Oct. 30, 2019	1.2	Add current DAC information	1,3,4,13
Jun. 28, 2019	1.1	Available information update, remove available item in section 1.	3
Jan. 07, 2019	1.0	Original	18