32768Hz Crystal Start-up OSC.

1. Introduction

In general, there are two oscillator options to be chosen for 32KHz clock source: R-OSC or 32768Hz crystal. For R-OSC, it is a low cost solution and only requires a resistor inside internal circuitry, but a lower time accuracy. For 32768Hz crystal, a higher time accuracy and higher cost option which requires a 32768Hz crystal with two bypass capacitors. These two options are used based on the user's applications needs and we will discuss more about this in the following sections.

2. Analysis

The following table lists the pros and cons for ROSC 32K vs. Crystal 32K.

	PROS	CONS
ROSC 32K	1. Less components, lower cost. 2. Fast start-up oscillation	1. Lower Time Accuracy
Crystal 32K	1. Higher Time Accuracy	1. More components, higher cost. 2. Slow start-up oscillation

As the list above, we know 32768Hz crystal has a slow start-up issue in nature. we will discuss more about this in this application note.

2.1 A successful 32768Hz Crystal Start-up

In order to have a successful 32768Hz crystal start-up oscillation, we should pay attention to two factors: Load capacitance (CL) and Equivalent Series Resistance (ESR). These two factors are normally indicated in 32768Hz crystal's specification. A larger CL and ESR will reduce the crystal's oscillation capability, even fail to oscillate. Thus, ESR should be selected properly; 20KΩ~100KΩ is recommended. When 32768Hz crystal is unable to oscillate, try a lower ESR 32768Hz crystal. The CL means the optimized loading capacitance work with 32768Hz crystal. We can calculate the loading capacitance from the MCU and 32768Hz crystal circuitry. Please refer to Fig. 1.

The capacitance is indicated as follows, Fig. 1

Cel: Shunt capacitance in parallel with 32768Hz crystal

Cp: Parasitic capacitance on PCB route

Cil: Equivalent capacitance inside MCU AMP.

$$\text{CL's equivalent capacitance} = \frac{(\text{Cel}+\text{Cp}+\text{Cil})_{X32I} \bullet (\text{Cel}+\text{Cp}+\text{Cil})_{X32O}}{(\text{Cel}+\text{Cp}+\text{Cil})_{X32I} + (\text{Cel}+\text{Cp}+\text{Cil})_{X32O}}$$

Suppose the capacitance on X32I and X32O are equivalent and symmetrical, then CL = (Cel+Cp+Cil) /2

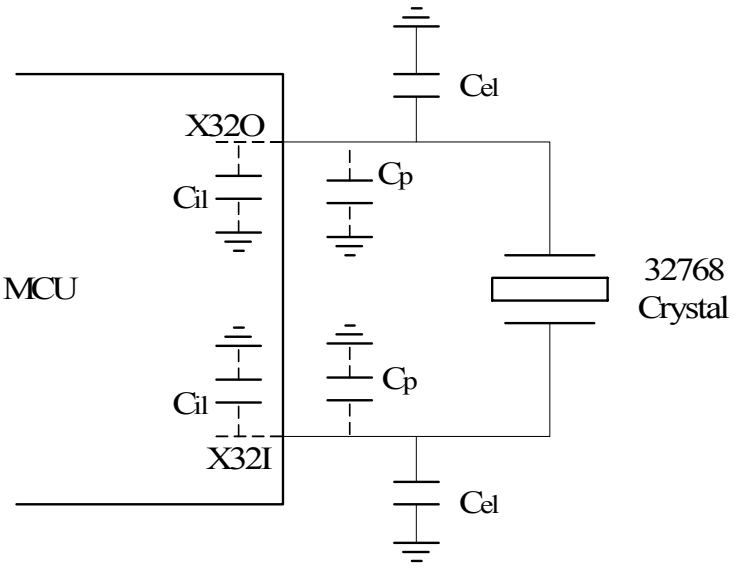


Fig.1: MCU & 32768Hz crystal

Here, we recommend CL ≦ 32768Hz crystal CL spec. value. The (Cil + Cp) can be measured by equipment and user is welling to make adjustment to the bypass capacitance Cel..

2.2 32768Hz Crystal Start-up Time

In Fig. 2, it requires a period of time from power on to 32768Hz crystal start-up, which may be varied, 10ms ~ 1 second. The time from 32768Hz crystal start-up to the maximum amplitude also varies. The factors that affect 32768Hz crystal start-up are:

- Higher 32768Hz crystal ESR is, slower start-up is.
- The larger 32768Hz crystal CL is, slower start-up is.
- Higher driving capability of MCU OSC apmlifer is, faster 32768Hz crystal start-up is. This will enhance the 32768Hz crystal's start capability.
- More power stored in CL, the faster crystal start-up is. It means the turn-over start-up of 32768Hz crystal will be faster than that of the first power-on or a long time start-up. This may be a factor that causes various start-up time each time in operating (In rapid turn-over oscillation, time can be as short as 10ms)

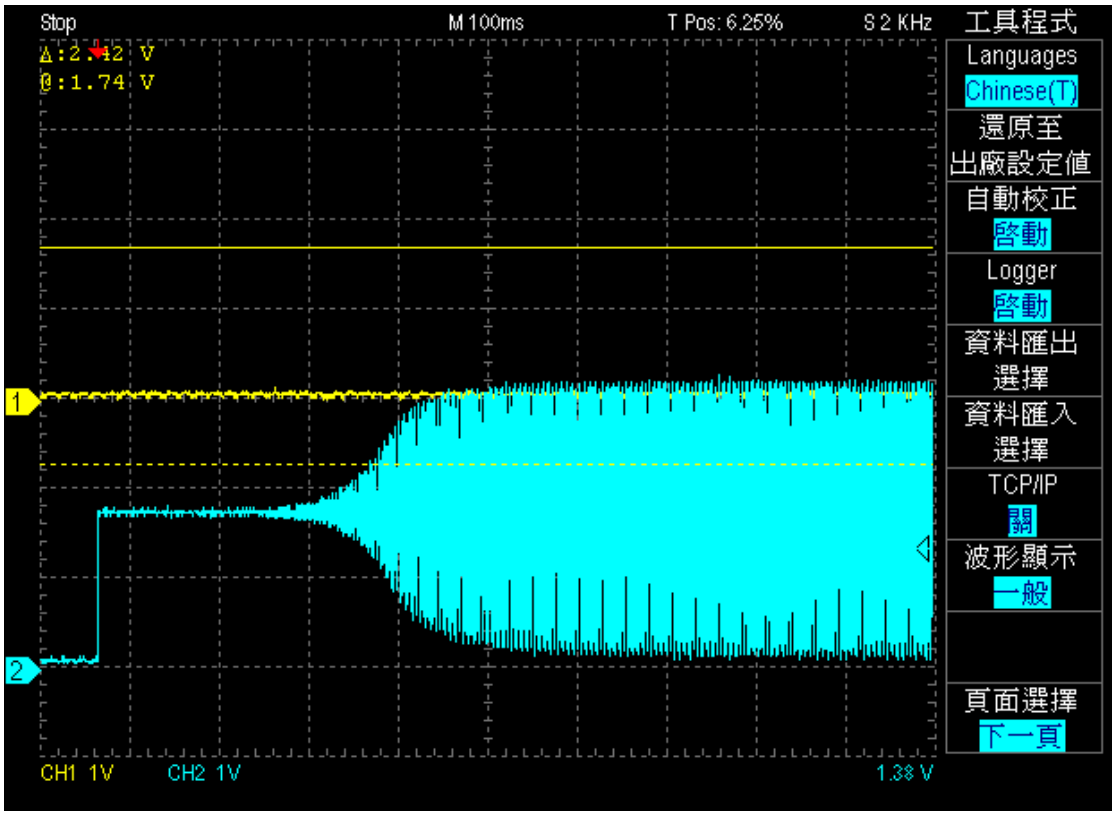


Fig. 2: 32768Hz crystal start-up waveform

2.3 Effect of Slow 32768Hz Crystal Start-up OSC

Most Generalplus's MCU involves high-frequency system clock (CPU clock) and 32K clock. These two clocks may vary in variety of MCU series. Examples are given as follows:

- When MCU has system clock and 32KHz clock work independently: note that 32KHz OSC starts oscillating slowly under this circumstances.
- When MCU 32K clock is derived from system clock by division: The effect caused by slow 32KHz clock start-up does not take into account.
- When system clock is PLL (phase lock loop): In general, PLL will multiply the 32K clock frequency. Note it may cause the 32kHz start-up oscillating slower.

Two out of three conditions are applying 32768Hz crystal for 32KHz clock source. We will discuss more about this in the following section.

2.3.1 When system clock and 32K clock operate independently

Under this infrastructure, the system clock start-up is faster than 32K OSC. That is, after system clock starts and CPU starts executing program, 32K OSC has not yet started oscillating. All functions related to the 32K clock sources, at this moment, are unable to operate. Thus, programmer must pay attention to this constrain when developing an application.

2.3.2 When system clock is PLL

When system clock is PLL, system clock is the base frequency of 32K clock. Thus, system activation is synchronized with 32K clock OSC and therefore, system clock (PLL) will start up slowly under power on or standby mode. Moreover, the 32K clock OSC requires a period of time to be stabilized before operation, it will cause system clock unstable during this period. Under this circumstance, we recommend CPU should avoid executing complex functions during the unstable period. On possible solution to resolve this issue is by using a polling mechanism to wait until clock to be stabilized. We will discuss this more about this in the next section.

3. Conclusion

Here, we conclude:

- In addition to a matching CL is able to obtain a precise 32768Hz frequency, 32768Hz crystal is welling to be activated normally as well. The factors that affect 32768Hz crystal include CL, ESR, and MCU's amplifier driving capability to 32768Hz crystal.
- User must be aware of the nature of slow 32768Hz crystal start-up. We highly recommend user should wait till 32K clock to be stabilized before proceeding any functions associated with 32KHz clock. Furthermore, under PLL clock infrastructure, we recommend the following method to wait for a stabilized 32KHz: After system is activated, turn on the Timebase 128Hz (derived from 32K clock source), interrupt and perform polling 128Hz twice to assure 32KHz is stabilized before executing other functions.