DATA SHEET

GPCE4XXXX

16-bit Sound Controller

Jun. 26, 2017

Version 1.1

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16-BIT SOUND CONTROLLER

1 GENERAL DESCRIPTION

GPCE4xxxx, a 16-bit architecture sound controller with USB interface, features the newest 16-bit microprocessor, *μ'nSP2.0*™ (pronounced as *micro-n-SP 2.0*). This high processing speed assures the *μ'nSP2.0*™ is capable of handling complex digital signal processes easily and rapidly. Therefore, GPCE4xxxx is applicable for the areas of digital sound process and voice recognition. The operating voltage of 2.4V through 5.5V and speed up to 48MHz yield the GPCE4xxxx to be easily used in varieties of applications. The memory capacity includes ROM (or OTP) plus a 4K-word working SRAM and 2K-word Cache RAM (also can be working RAM). Other features including 48 programmable multi-functional I/Os, five 16-bit timers/counters, 32768Hz Real Time Clock, Low Voltage Reset/Detection, eight channels 12-bit ADC (one channel built-in MIC amplifier with auto gain controller), capacitive touch sensor, one SPI flash controller, one 16-bit DAC with push-pull amplifier and many others.

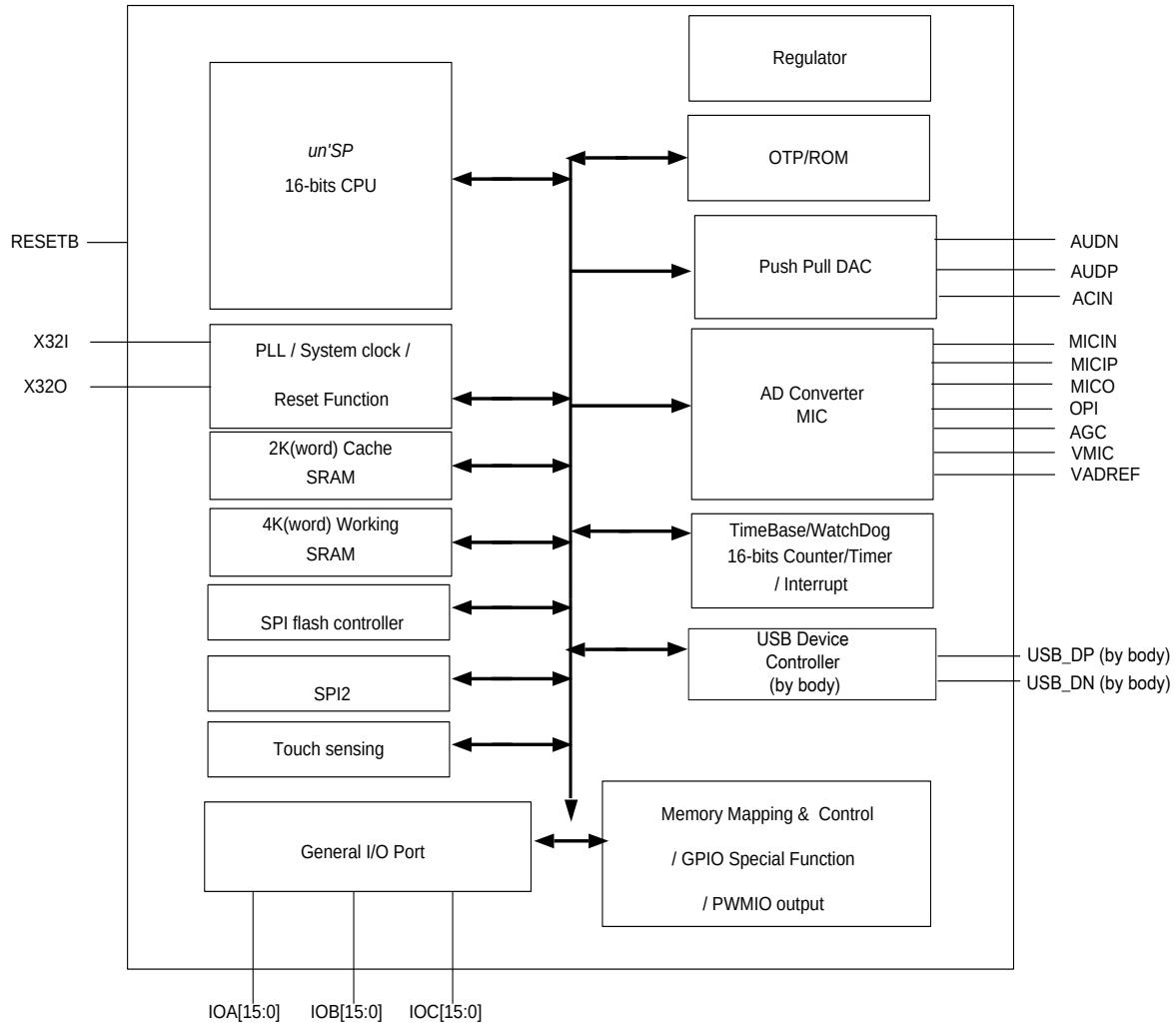
2 FEATURES

- 16-bit *μ'nSP2.0*™ microprocessor
- CPU Clock: max. 48MHz
- Operating Voltage: 2.4V - 5.5V
- Power regulator built-in with input voltage: 2.4~5.5V, output voltage: 2.4~3.3V
- IO PortA & B & C Operating Voltage: 2.4V - 5.5V
- Fast speed OTP or ROM (by body)
- 4K-word working SRAM
- 2K-word cache SRAM (also can be released to working-RAM)
- Total 384-byte buffer RAM
- Software-based audio processing
- Two sets of 14-bit software channel with noise filter, mixer and scalar to play high quality sound
- Standby mode for power saving
- Total five 16-bit timers, including three general-purpose 16-bit timers/counters, two touch-sensing timers (also can released for general-purpose use).
- One 14-bit DAC with push-pull amplifier. Supports cascade mode as well as stereo mode
- 48 general I/Os (bit programmable)
- Key wakeup function (IOA0 - 15, IOB0-15, IOC0-15)
- Capacitor touch-sensing hardware for 48 I/O
- PLL feature for system clock
- 32768Hz Real Time Clock (RTC), crystal or internal resistor oscillator selected.
- Eight channels 12-bit AD converter, Built-in microphone amplifier and AGC or PGA function selected
- Low voltage reset and low voltage detection
- Watchdog Enable (option)
- Two SPI serial interface I/Os. One is SPI flash controller which supports one-I/O, two-I/O, four-I/O modes and support auto read/program mode. The other is normal SPI interface.
- Supports USB 2.0 full speed (12MHz) compliant device with built-in transceiver (by body option)

3 APPLICATION FIELD

- Voice Recognition Products
- Intelligent Interactive Talking Toys
- Advanced Educational Toys
- Kids Learning Products
- Kids Storybook
- General Speech Synthesizer
- Long Duration Audio Products
- Recording / Playback Products

4 BLOCK DIAGRAM



5 GPCE4XXXX SERIES AND DIFFERENT FEATURES LIST

Body	GPCE4P096UA	GPCE4096UA	GPCE4096A	GPCE4064A
Working Voltage	2.4~5.5V	2.4~5.5V	2.4~5.5V	2.4~5.5V
Max. CPU clock	48MHz	48MHz	48MHz	48MHz
RAM Size	6K-Word (include cache)	6K-Word (include cache)	6K-Word (include cache)	6K-Word (include cache)
Cache Size	2K-Word	2K-Word	2K-Word	2K-Word
ROM/OTP type	OTP	ROM	ROM	ROM
ROM/OTP Size	48K-Word	48K-Word	48K-Word	32K-Word
IO Port	48 (IOA/B/C)	48 (IOA/B/C)	48 (IOA/B/C)	48 (IOA/B/C)
SPI	2	2	2	2
USB Device Controller	Yes	Yes	No	No

6 SIGNAL DESCRIPTIONS

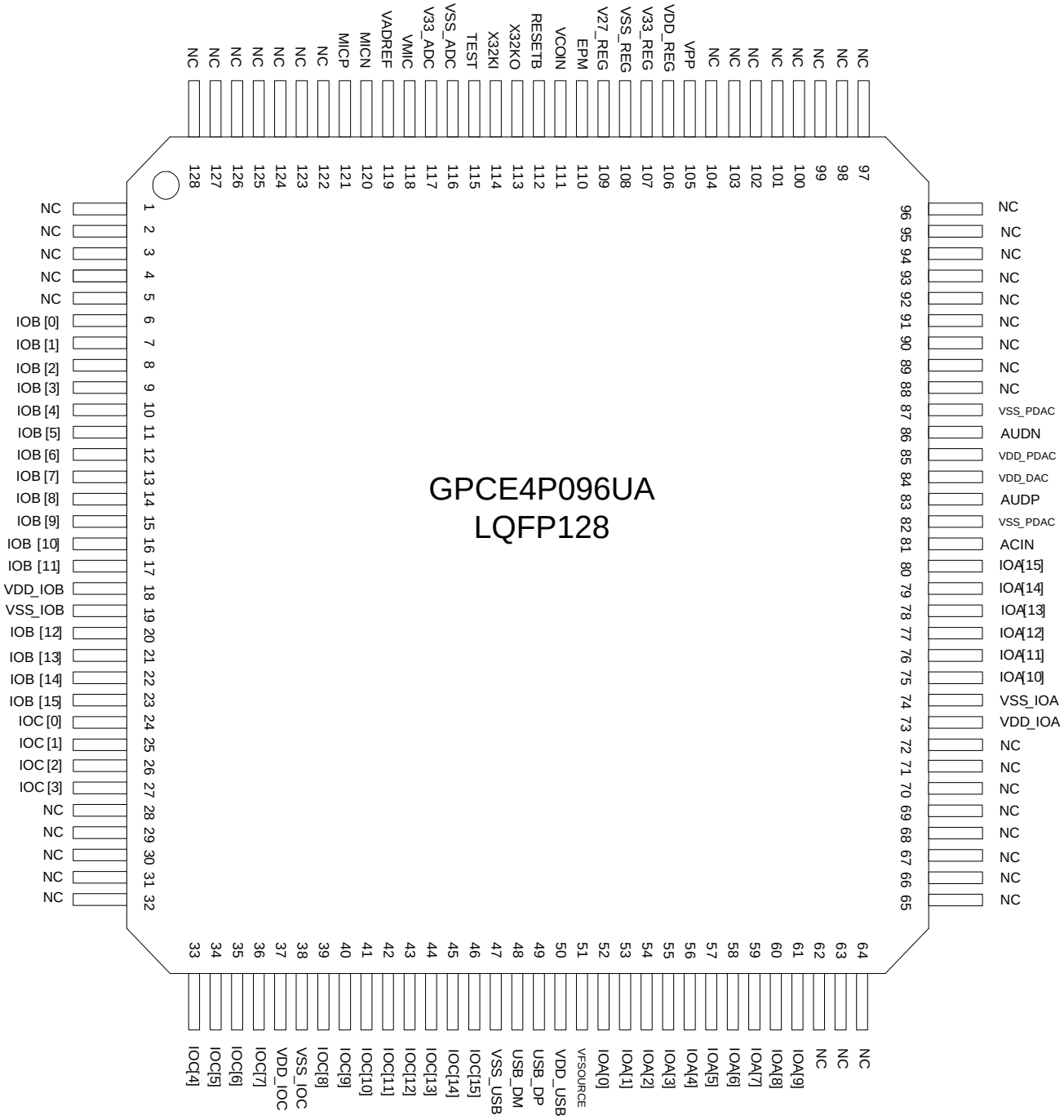
6.1 GPCE4P096UA

6.1.1 Pin descriptions

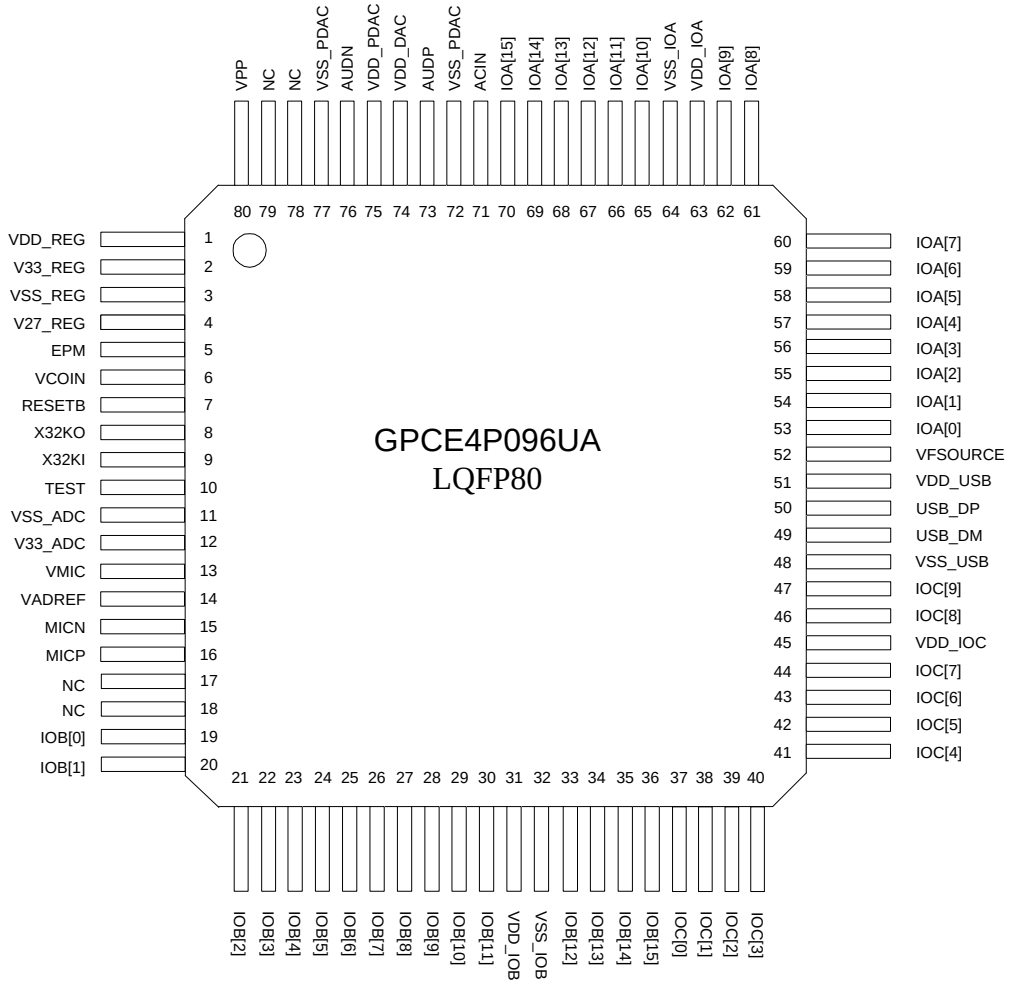
Mnemonic	Type	Description
PORT A, Port B		
IOA [15:0]	I/O	IOA[15:0]: bi-directional I/O ports It can be programmed as wakeup I/O pins.
IOB [15:0]	I/O	IOB [15:0]: bi-directional I/O ports. IOB[15] is shared with serial data port of OTP controller IOB[14] is shared with serial clock input port of OTP controller It can be programmed as wakeup I/O pins. IOB[11] is shared with ADC OP AMP output IOB[10] is shared with (OPI) ADC MIC amplifier output (refer to application circuit) IOB[9] is shared with ADC OPI Audio amplifier negative input (refer to application circuit) IOB[8] is shared with ADC AGC by pass filter (refer to application circuit)
IOC [15:0]	I/O	IOC [15:0]: bi-directional I/O ports. It can be programmed as wakeup I/O pins.
Power & GND		
VDD_IOA	P	Power VDD for Port A
VSS_IOA	G	Power GND for Port A
VDD_IOB	P	Power VDD for Port B
VSS_IOB	G	Power GND for Port B
VDD_IOC	P	Power VDD for Port C
VSS_IOC	G	Power GND for Port C
V33_ADC	P	Power VDD for AD (3.3V)
VSS_ADC	G	Power GND for AD
V33_REG	P	3V Power output from regulator
V27_REG	P	2.7V Power output from regulator
VDD_REG	P	Power supply for regulator (2.4V~5.5V)
VSS_REG	G	Ground reference for regulator
VDD_DAC	P	Positive 5V supply for push-pull DAC
VDD_PDAC	P	Positive 5V supply for push-pull DAC post driver
VSS_PDAC	G	Ground reference for push-pull DAC post driver
VDD_USB	P	Power for USB
VSS_USB	G	Ground for USB
CLK SYSTEM/ ICE INTERFACE		
X32KI	I	32K Oscillator crystal input/ R32K OSCI
X32KO	O	32K Oscillator crystal output
OPTION		
TEST	I	TEST Mode selection pin, high is test mode and low is normal mode (Pad internal pull low)
DAC		
AUDP	O	Audio output of push pull DAC
AUDN	O	Audio output of push pull DAC
ACIN	U	Audio analog mixer in
ADC		

Mnemonic	Type	Description
MICP	I	MIC amplifier input positive (Internal Floating)
MICN	I	MIC amplifier input negative (refer to application circuit)
VMIC	O	Microphone power supply
VADREF	O	AVREF_DA reference pin
PLL		
VCOIN	I	PLL6M low pass filter input
Other Signal		
RESETB	I	System reset pin (active low) (internal 47Kohm pull high resistor)
VPP	I	OTP program VPP pin
EPM	I	Program enable pin
USB		
USB_DP	I/O	USB DP pin of USBPHY
USB_DM	I/O	USB DM pin of USBPHY
Auto Trim FUSE		
VFSOURCE	I	Trimming Power PAD for IROSC6M

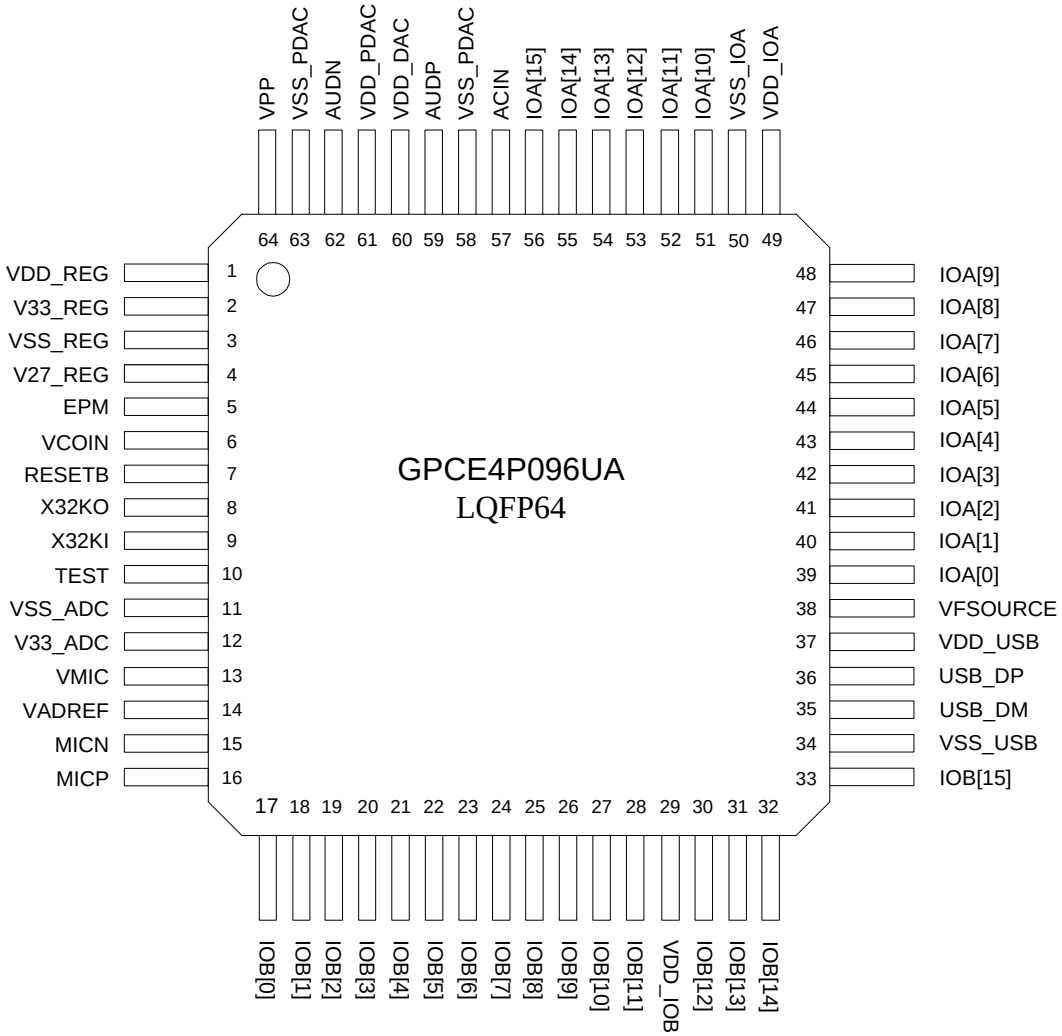
6.1.2 LQFP128 Package Pin Assignment



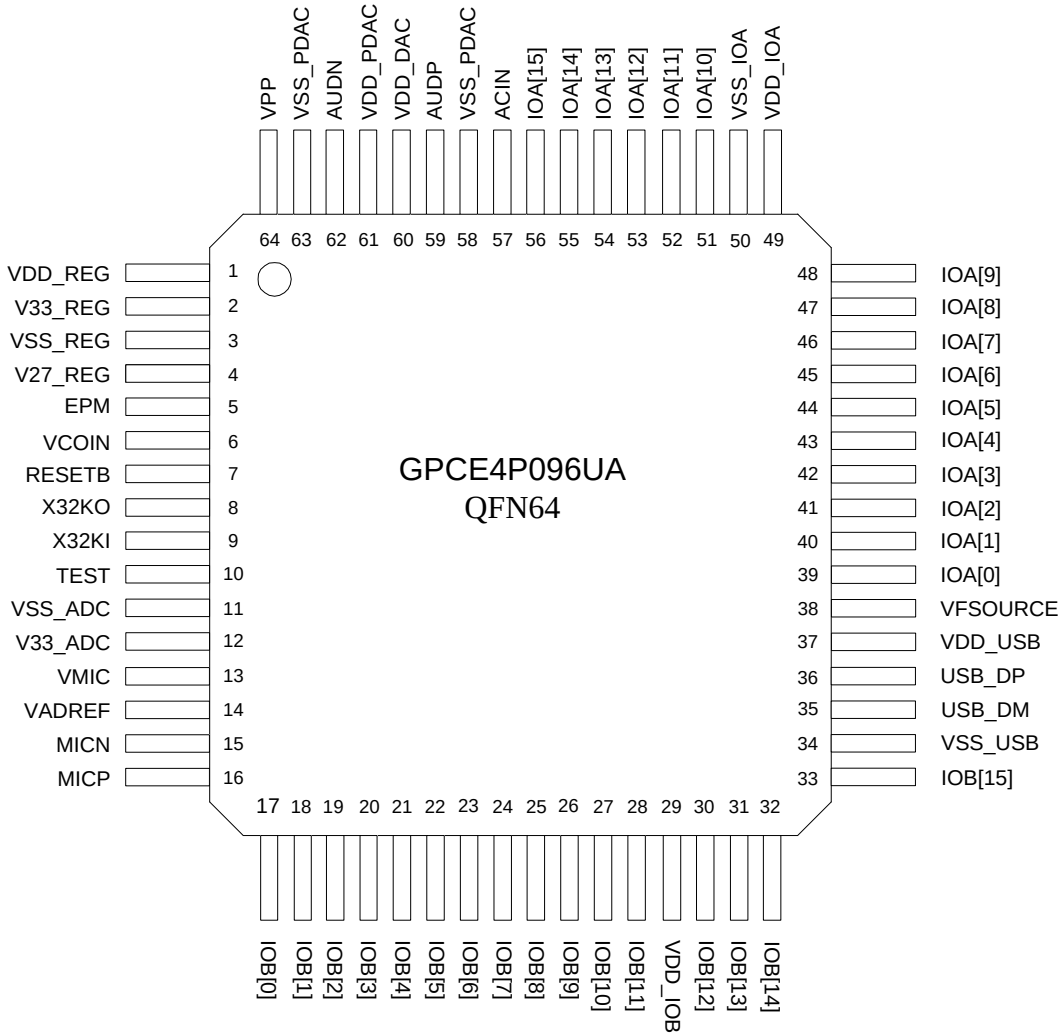
6.1.3 LQFP80 Package Pin Assignment



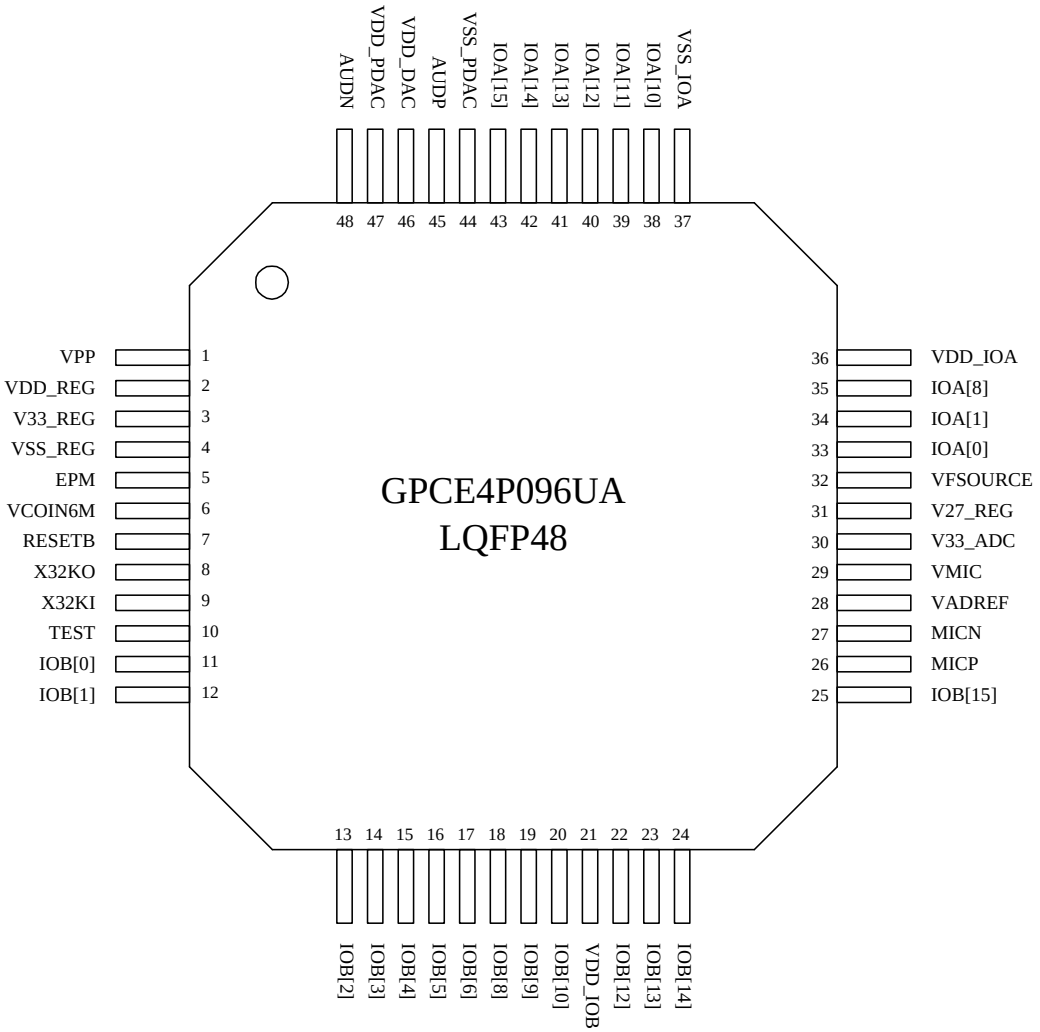
6.1.4 LQFP64 Package Pin Assignment



6.1.5 QFN64 Package Pin Assignment



6.1.6 LQFP48 Package Pin Assignment



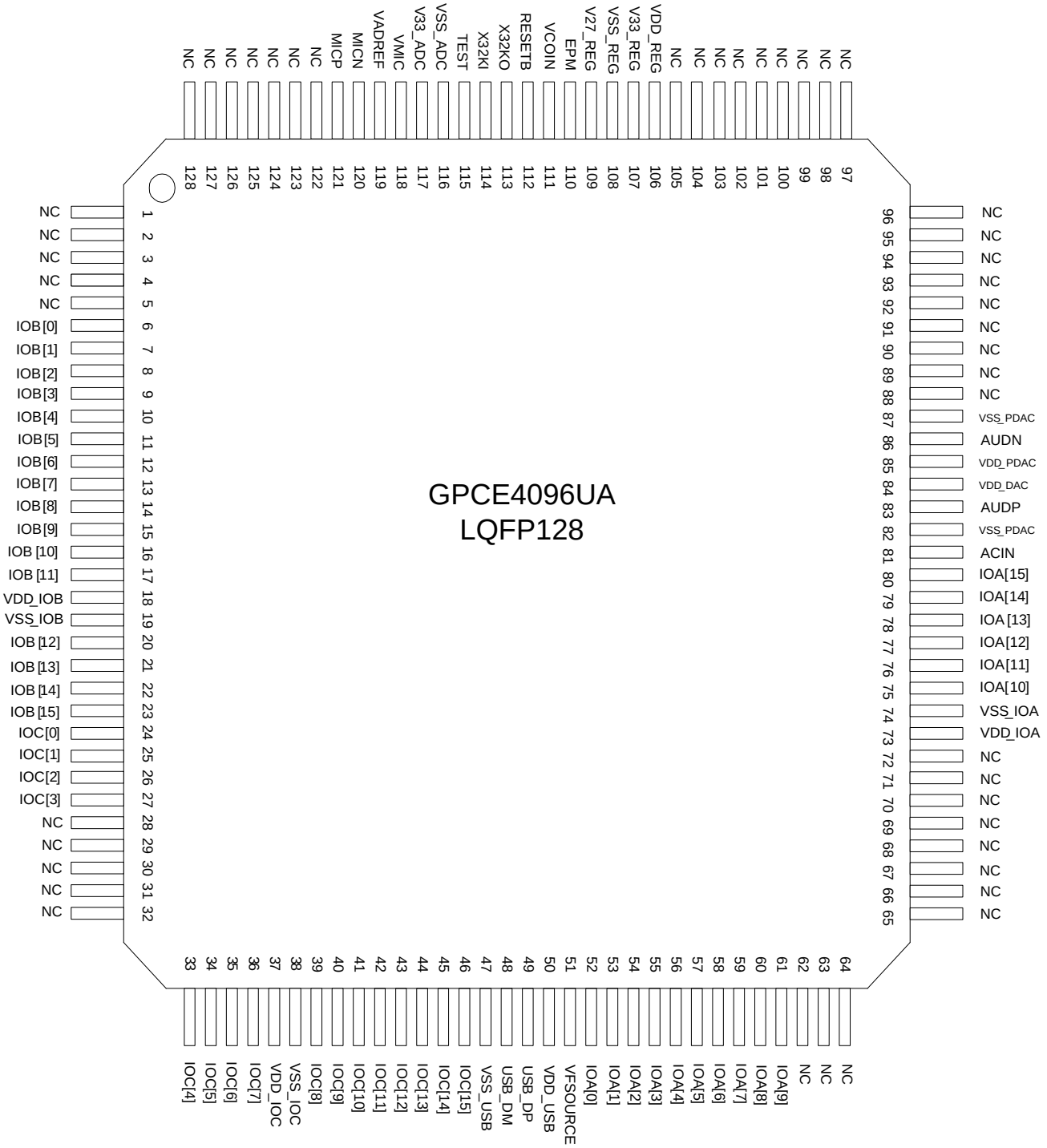
6.2 GPCE4096UA

6.2.1 Pin descriptions

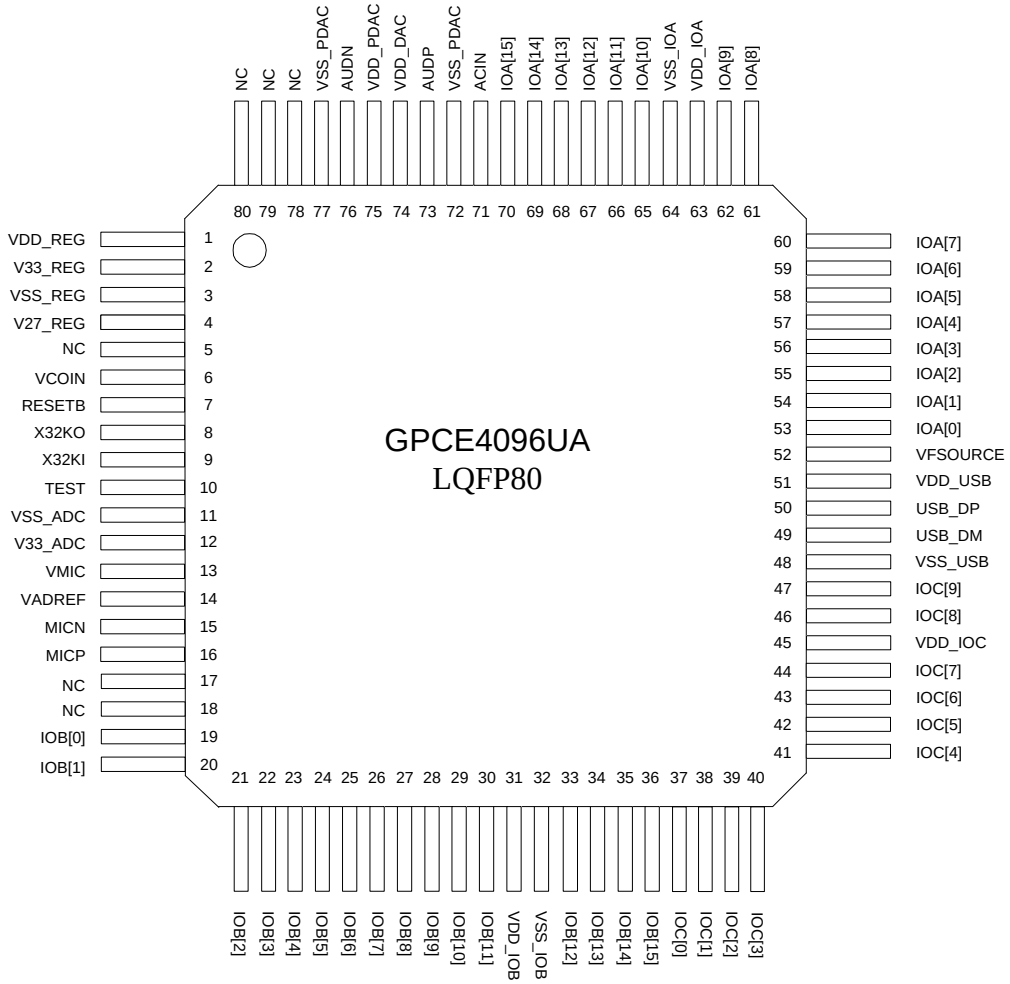
Mnemonic	Type	Description
PORT A, Port B		
IOA [15:0]	I/O	IOA[15:0]: bi-directional I/O ports It can be programmed as wakeup I/O pins.
IOB [15:0]	I/O	IOB [15:0]: bi-directional I/O ports. It can be programmed as wakeup I/O pins. IOB[11] is shared with ADC OP AMP output IOB[10] is shared with (OPI) ADC MIC amplifier output (refer to application circuit) IOB[9] is shared with ADC OPI Audio amplifier negative input (refer to application circuit) IOB[8] is shared with ADC AGC by pass filter (refer to application circuit)
IOC [15:0]	I/O	IOC [15:0]: bi-directional I/O ports. It can be programmed as wakeup I/O pins.
Power & GND		
VDD_IOA	P	Power VDD for Port A
VSS_IOA	G	Power GND for Port A
VDD_IOB	P	Power VDD for Port B
VSS_IOB	G	Power GND for Port B
VDD_IOC	P	Power VDD for Port C
VSS_IOC	G	Power GND for Port C
V33_ADC	P	Power VDD for AD (3.3V)
VSS_ADC	G	Power GND for AD
V33_REG	P	3V Power output from regulator
V27_REG	P	2.7V Power output from regulator
VDD_REG	P	Power supply for regulator (2.4V~5.5V)
VSS_REG	G	Ground reference for regulator
VDD_DAC	P	Positive 5V supply for push-pull DAC
VDD_PDAC	P	Positive 5V supply for push-pull DAC post driver
VSS_PDAC	G	Ground reference for push-pull DAC post driver
VDD_USB	P	Power for USB
VSS_USB	G	Ground for USB
CLK SYSTEM/ ICE INTERFACE		
X32KI	I	32K Oscillator crystal input/ R32K OSCI
X32KO	O	32K Oscillator crystal output
OPTION		
TEST	I	TEST Mode selection pin, high is test mode and low is normal mode (Pad internal pull low)
DAC		
AUDP	O	Audio output of push pull DAC
AUDN	O	Audio output of push pull DAC
ACIN	U	Audio analog mixer in
ADC		
MICP	I	MIC amplifier input positive (Internal Floating)
MICN	I	MIC amplifier input negative (refer to application circuit)
VMIC	O	Microphone power supply

Mnemonic	Type	Description
VADREF	O	AVREF_DA reference pin
PLL		
VCOIN	I	PLL6M low pass filter input
Other Signal		
RESETB	I	System reset pin (active low) (internal 47Kohm pull high resistor)
USB		
USB_DP	I/O	USB DP pin of USBPHY
USB_DM	I/O	USB DM pin of USBPHY
Auto Trim FUSE		
VFSOURCE	I	Trimming Power PAD for IROSC6M

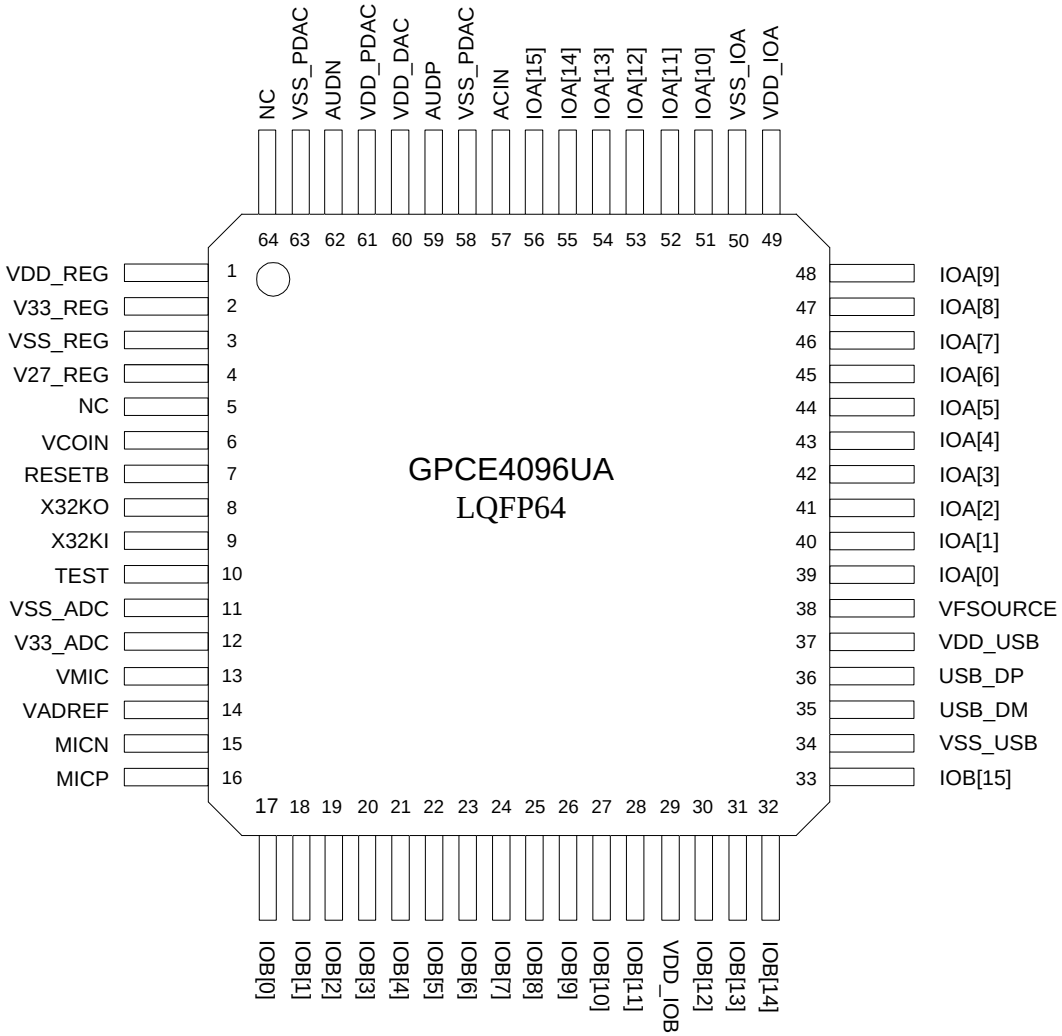
6.2.2 LQFP128 Package Pin Assignment



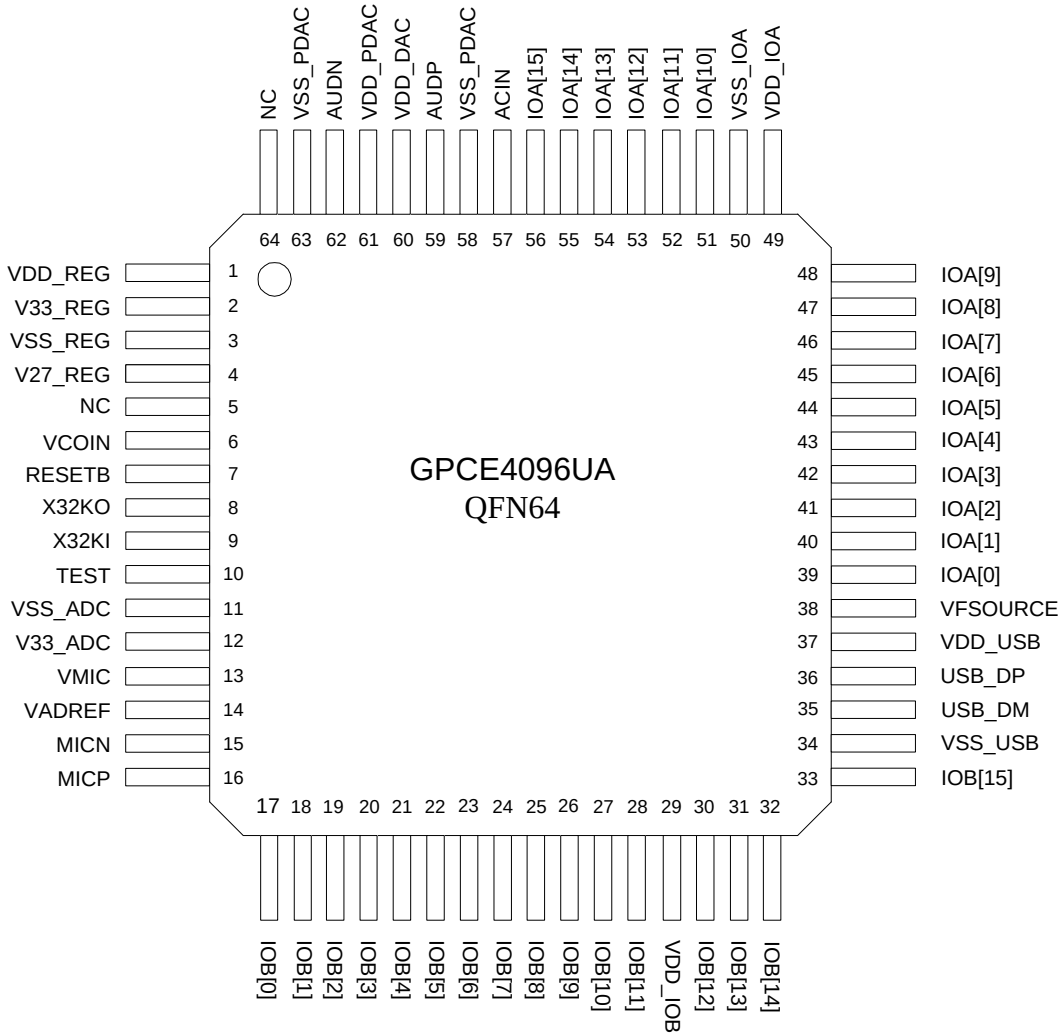
6.2.3 LQFP80 Package Pin Assignment



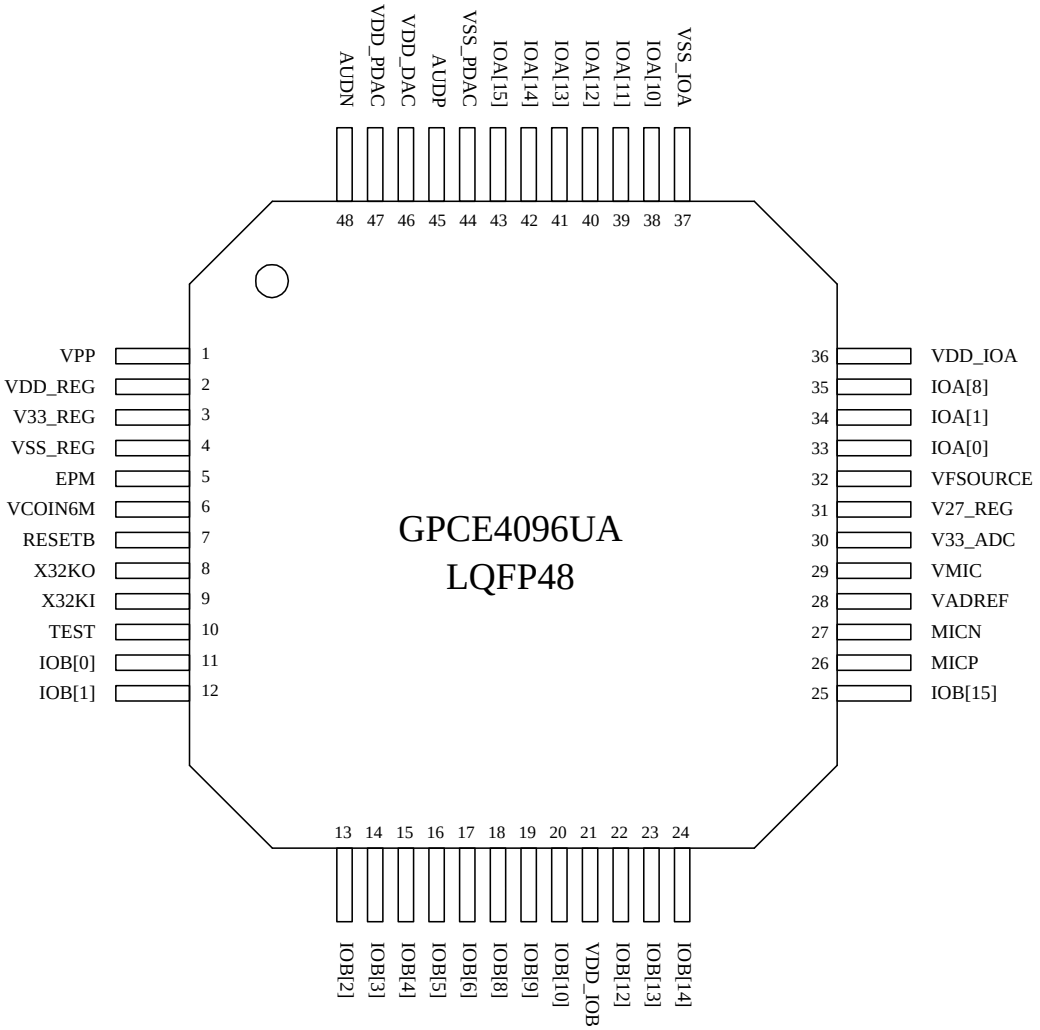
6.2.4 LQFP64 Package Pin Assignment



6.2.5 QFN64 Package Pin Assignment



6.2.6 LQFP48 Package Pin Assignment



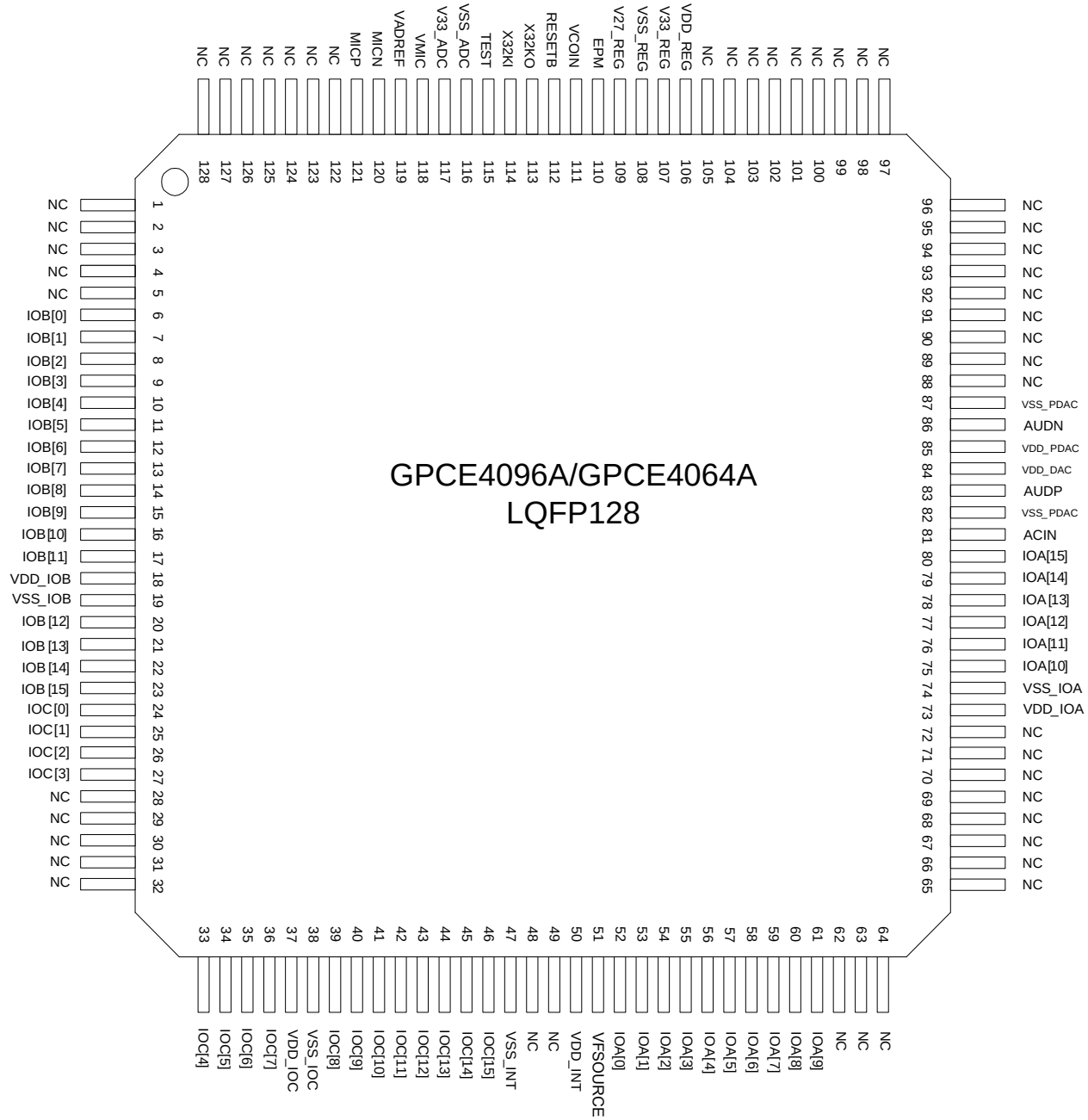
6.3 GPCE4096A/GPCE4064A

6.3.1 Pin descriptions

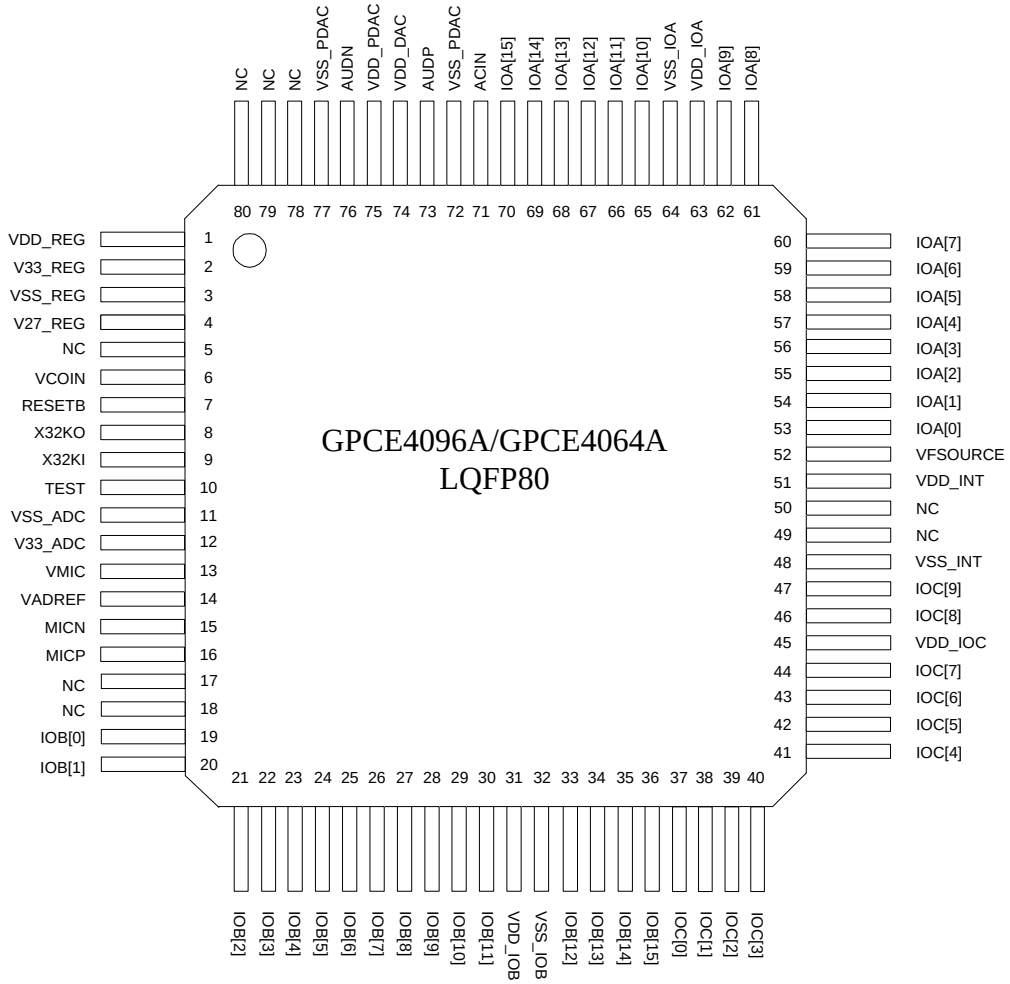
Mnemonic	Type	Description
PORT A, Port B		
IOA [15:0]	I/O	IOA[15:0]: bi-directional I/O ports It can be programmed as wakeup I/O pins.
IOB [15:0]	I/O	IOB [15:0]: bi-directional I/O ports. It can be programmed as wakeup I/O pins. IOB[11] is shared with ADC OP AMP output IOB[10] is shared with (OPI) ADC MIC amplifier output (refer to application circuit) IOB[9] is shared with ADC OPI Audio amplifier negative input (refer to application circuit) IOB[8] is shared with ADC AGC by pass filter (refer to application circuit)
IOC [15:0]	I/O	IOC [15:0]: bi-directional I/O ports. It can be programmed as wakeup I/O pins.
Power & GND		
VDD_IOA	P	Power VDD for Port A
VSS_IOA	G	Power GND for Port A
VDD_IOB	P	Power VDD for Port B
VSS_IOB	G	Power GND for Port B
VDD_IOC	P	Power VDD for Port C
VSS_IOC	G	Power GND for Port C
V33_ADC	P	Power VDD for AD (3.3V)
VSS_ADC	G	Power GND for AD
V33_REG	P	3V Power output from regulator
V27_REG	P	2.7V Power output from regulator
VDD_REG	P	Power supply for regulator (2.4V~5.5V)
VSS_REG	G	Ground reference for regulator
VDD_DAC	P	Positive 5V supply for push-pull DAC
VDD_PDAC	P	Positive 5V supply for push-pull DAC post driver
VSS_PDAC	G	Ground reference for push-pull DAC post driver
VDD_INT	P	Power for internal block
VSS_INT	G	Ground for internal block
CLK SYSTEM/ ICE INTERFACE		
X32KI	I	32KHz Oscillator crystal input/ R32K OSCI
X32KO	O	32KHz Oscillator crystal output
OPTION		
TEST	I	TEST Mode selection pin, high is test mode and low is normal mode (Pad internal pull low)
DAC		
AUDP	O	Audio output of push pull DAC
AUDN	O	Audio output of push pull DAC
ACIN	U	Audio analog mixer in
ADC		
MICP	I	MIC amplifier input positive (Internal Floating)
MICN	I	MIC amplifier input negative (refer to application circuit)
VMIC	O	Microphone power supply

Mnemonic	Type	Description
VADREF	O	AVREF_DA reference pin
PLL		
VCOIN	I	PLL6M low pass filter input
Other Signal		
RESETB	I	System reset pin (active low) (internal 47Kohm pull high resistor)
Auto Trim FUSE		
VFSOURCE	I	Trimming Power PAD for IROSC6M

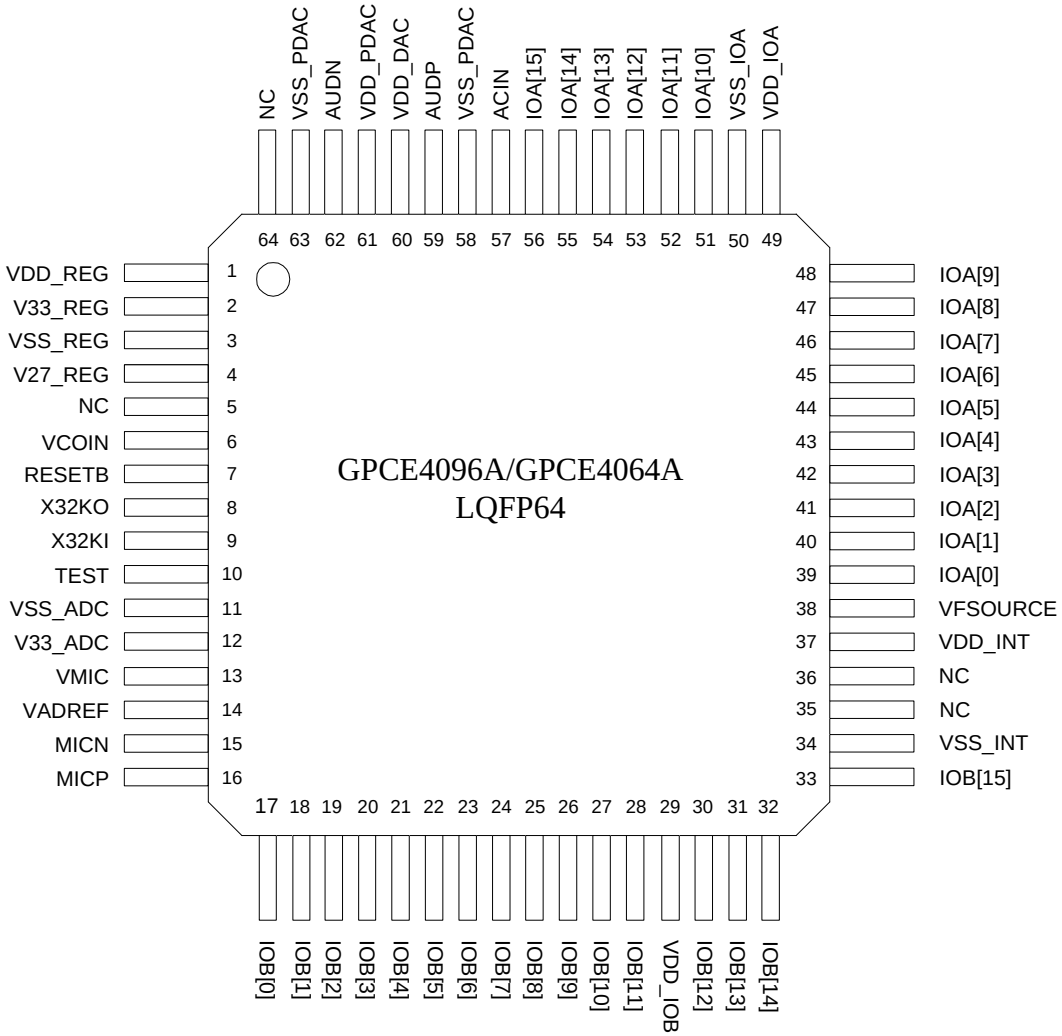
6.3.2 LQFP128 Package Pin Assignment



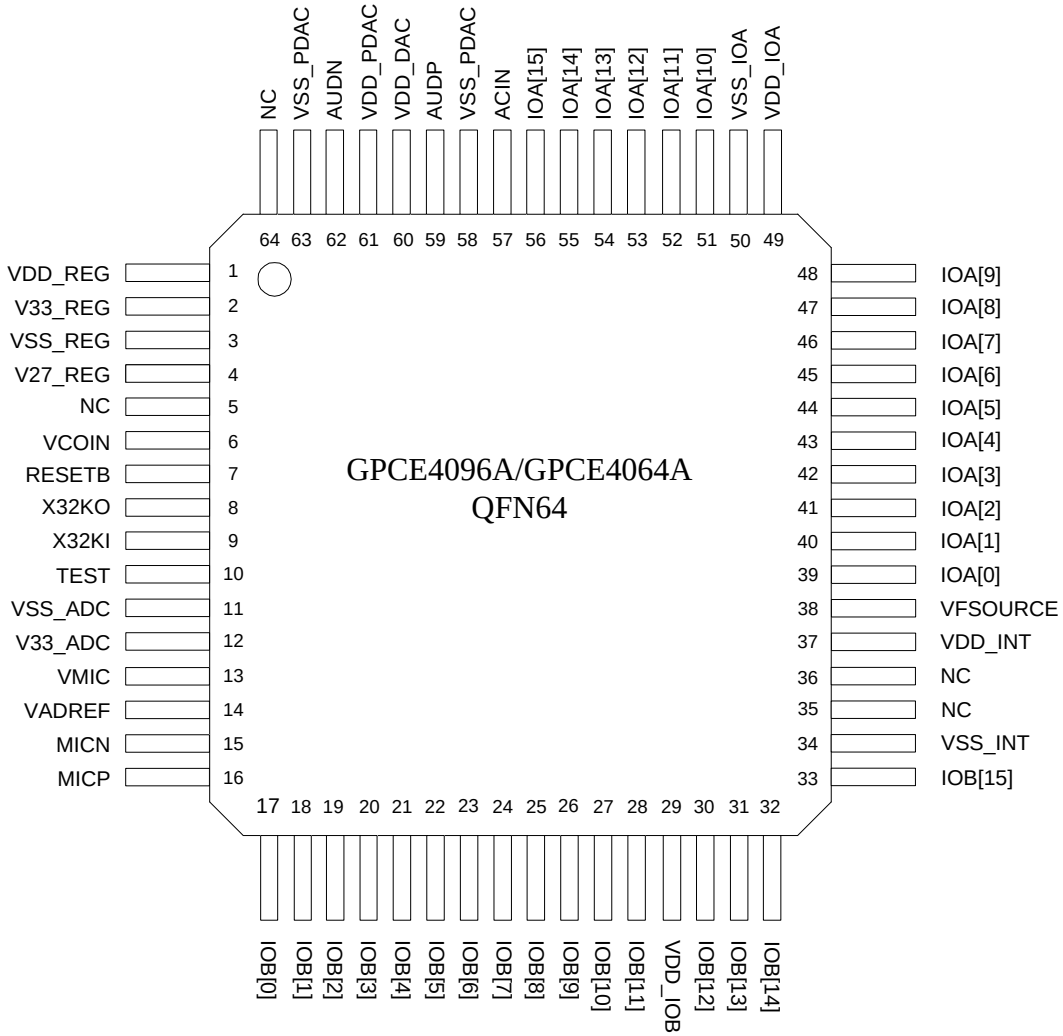
6.3.3 LQFP80 Package Pin Assignment



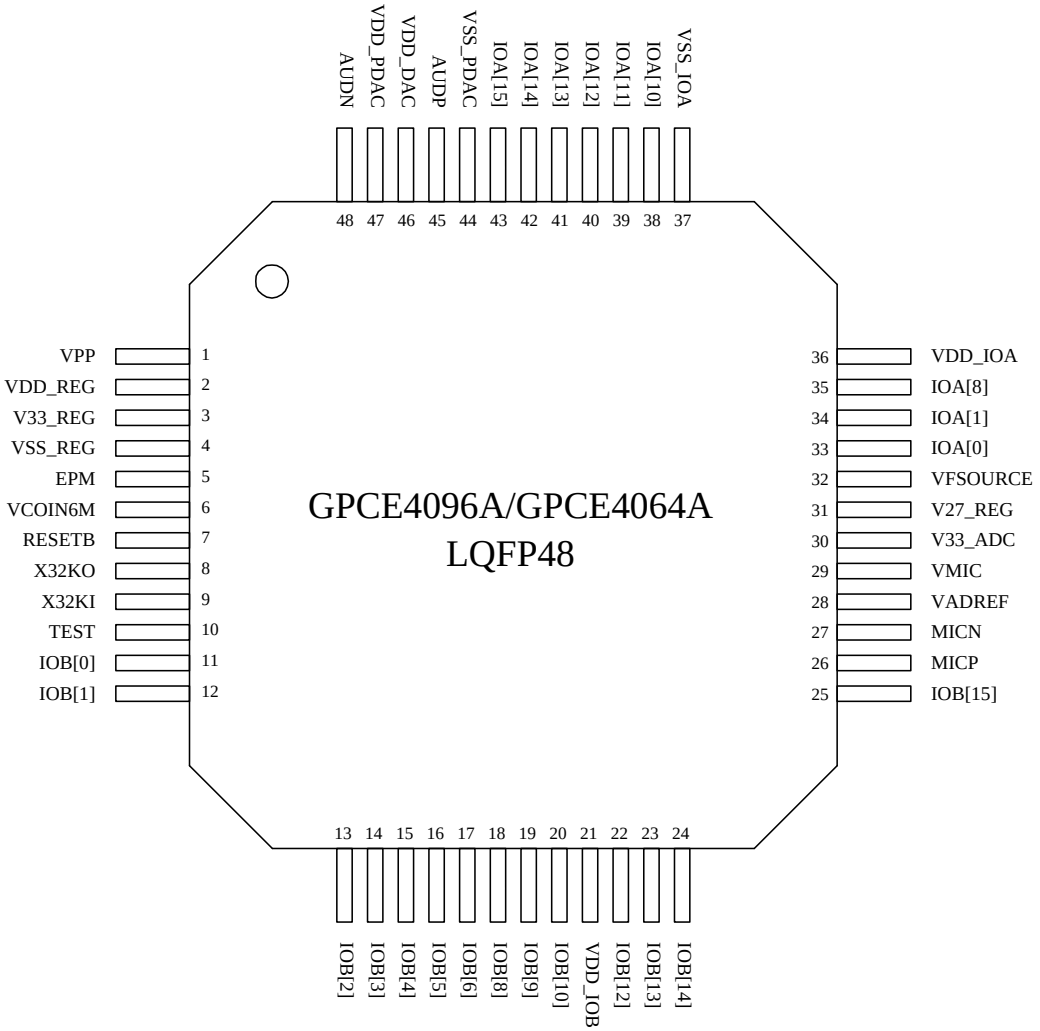
6.3.4 LQFP64 Package Pin Assignment



6.3.5 QFN64 Package Pin Assignment



6.3.6 LQFP48 Package Pin Assignment



7 FUNCTION DESCRIPTIONS

7.1 CPU

The GPCE4xxxx is equipped with a 16-bit μ'nS2.0P™ (pronounced as micro-n-SP). Sixteen registers are featured in μ'nSP™ 2.0: R1 - R4 and R8 ~ R15 (General- purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP) , SR (Segment Register) and eight extended registers. The interrupts include 23 FIQs (Fast Interrupt Request) and IRQs (Interrupt Request), plus one software-interrupt, BREAK.

7.2 Memory

7.2.1 SRAM

There are 4K-word working SRAM and 2K-word Cache RAM (also can be working RAM), ranged from $0000 through $17FF.

7.2.2 OTP

GPCE4xxxx features a high-speed memory with access speed of three CPU clock cycles.

7.3 PLL, Clock, Power Mode

7.3.1 PLL (Phase Lock Loop)

The purpose of PLL is to provide a base frequency (32768Hz) and to pump the frequency from 6MHz to 48MHz for system clock (F_{OSC}). The default PLL frequency is 12MHz.

7.3.1.1 System clock

Basically, the system clock is provided by PLL and programmed by the Port_SystemClock (R/W) to determine the clock frequency for system.

7.3.1.2 32768Hz RTC

The Real Time Clock (RTC) is normally used in watch, clock or other time related products. A 2Hz-RTC (0.5 seconds) function is loaded in GPCE4xxxx. The RTC counts the time as well as to wake CPU up whenever RTC occurs. Since the RTC is generated each 0.5 seconds, time can be tracked by the total number of RTC occurrences. In addition, GPCE4xxxx supports 32768Hz crystal oscillator in normal mode and auto-power-saving mode. In normal mode, 32768Hz OSC always runs at the highest power consumption. In auto-power-saving mode, however, it runs at normal mode for the first 7.5 seconds and switches back to power-saving mode automatically to save powers.

7.4 Standby Mode

The GPCE4xxxx features a power savings mode (or called standby mode) for low power applications. In such mode, SRAM and I/Os remain in the previous states until CPU being awakened. After GPCE4xxxx wakes up, CPU will continue to execute the program from where it slept.

7.5 Low Voltage Detection and Low Voltage Reset

7.5.1 Low voltage detection (LVD)

The Low Voltage Detection (LVD) reports the circumstance of present voltage. There are seven LVD levels to be selected: 2.4V, 2.6V, 2.8V, 3.0V, 3.2V, 3.4V, and 3.6V.

7.5.2 Low voltage reset

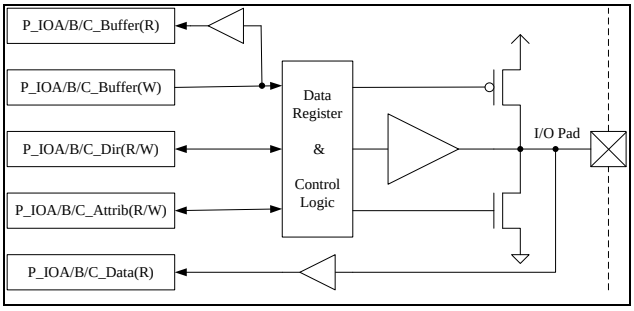
In addition to the LVD, GPCE4xxxx has another important function, Low Voltage Reset (LVR). With LVR function, a reset signal is generated to reset system when the operating voltage drops below LVR level.

7.6 Interrupt

The GPCE4xxxx has 25 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. User can refer programming guide for details.

7.7 I/O

The GPCE4xxxx has 48 bit-programmable I/Os. with programmable wakeup capability. The following diagram is an I/O schematic.



In addition to a general purpose I/O port function, IOA/B/C also shares/carries some special functions. A summary of IOA/B/C special functions is listed as follows:

7.8 Special Function in Port

Port	Special Function	Function Description	Note
IOA0	IO_PWM/ High driving I/O	IO_PWM Output	Refer to Timer section
IOA1	IO_PWM/ High driving I/O	IO_PWM Output	Refer to Timer section
IOA2	IO_PWM/ High driving I/O	IO_PWM Output	Refer to Timer section
IOA3	IO_PWM/ High driving I/O	IO_PWM Output	Refer to Timer section
IOA4	IROUT	IR Output	-
IOA5	-	-	-
IOA6	Feedback Input2	-	-
	EXT2	External interrupt source 2 (negative edge triggered)	Set IOA6 as floating input mode
IOA7	Feedback Output2	Work with IOA6 by adding a RC circuit between them to get an OSC to EXT2 interrupts	Set IOA7 as inverted output
IOA8	Feedback Input1	-	-
	EXT1	External interrupt source 1 (negative edge triggered)	Set IOA8 as floating input mode
IOA9	Feedback Output1	Work with IOA8 by adding a RC circuit between them to get an OSC to EXT1 interrupt	Set IOA9 as inverted output
IOA10	SPI IO3/ Fast driving I/O	SPI IO3	Refer to SPIFC section
IOA11	SPI IO2/ Fast driving I/O	SPI IO2	Refer to SPIFC section
IOA12	SPI CS/ Fast driving I/O	SPI chip select	Refer to SPIFC section
IOA13	SPI CK/ Fast driving I/O	SPI clock	Refer to SPIFC section
IOA14	SPI RX/ Fast driving I/O	SPI data input	Refer to SPIFC section
IOA15	SPI TX/ Fast driving I/O	SPI data output	Refer to SPIFC section
IOB0	AN0	ADC Channel 0	Refer to ADC section
IOB1	AN1	ADC Channel 1	Refer to ADC section
IOB2	AN2	ADC Channel 2	Refer to ADC section
IOB3	AN3	ADC Channel 3	Refer to ADC section
IOB4	AN4	ADC Channel 4	Refer to ADC section
IOB5	AN5	ADC Channel 5	Refer to ADC section
IOB6	AN6	ADC Channel 6	Refer to ADC section
IOB7	AN7	ADC Channel 7	Refer to ADC section
IOB8	AGC	ADC AGC	Refer to ADC section
IOB9	OPI	ADC OPI	Refer to ADC section
IOB10	MICOUT	ADC MICOUT	Refer to ADC section
IOB11	OPO	ADC OPO	Refer to ADC section
IOB12	SPI2 CS	SPI2 chip select	Refer to SPI2 section
IOB13	SPI2 CK	SPI2 clock	Refer to SPI2 section
IOB14	SPI2 RX	SPI2 data input	Refer to SPI2 section
IOB15	SPI2 TX	SPI2 data output	Refer to SPI2 section
IOA[15:0], IOB[15:0] IOC[15:0]	Touch sensing input	Touch sensing input	Refer to CTS section

7.9 Timer / Counter

The GPCE4xxxx has five 16-bit timer/counters. They are re-loaded up-counters. When timer overflows from $FFFF to $0000, the carry (overflow) signal will make the user's preset value to be loaded into timer automatically and count up again. At the same time, the carry signal will generate an interrupt signal if the corresponding bit is enabled.

7.9.1 IO PWM

One IO PWMs which duty is selected from 1/256 to 254/256. These PWM signals can be applied for controlling the speed of motor or other device.

7.9.2 Timebase

Timebase, generated by 32768Hz crystal oscillator, is a combination of frequency selection, generating 4KHz, 2KHz, 512Hz, 64Hz, 16Hz and 2Hz interrupt sources (FIQ6/IRQ6, FIQ7/IRQ7) for real-time-clock.

7.10 Capacitance Touch Sensor(CTS) and CTS Timers

GPCE4xxxx provides Capacitive Touch sensor. It is able to perform capacitive sensing, decision making, responsive actions and other duties pertinent to the system as well.

7.11 Sleep Mode, Wakeup, Halt Mode, and Watchdog

7.11.1 Sleep and wakeup modes

1) Sleep, Halt: After power-on reset, IC starts running until a sleep command is issued. When a sleep command is accepted, IC will turn the system clock (PLL) off. It enters sleep mode if 32KHz Sleep Status bit is cleared or enters halt mode if 32KHz Sleep Status bit is set.
2) Wakeup: CPU awaking from sleep mode requires a wakeup signal to turn the system clock (PLL) on. The FIQ/IRQ signal makes CPU to complete the wakeup process and initialization. The CPU wakeup source is given in the following table. Wakeup up source include all FIQ source and all interrupt source.

7.11.2 Watchdog Reset

If the watchdog function is enabled, a reset signal is generated to reset system when watchdog counter is overflow.

7.12 ADC (Analog to Digital Converter) / DAC

The GPCE4xxxx has eight channels 12-bit ADC (Analog to Digital Converter) to convert analog signal to digital signal. The eight channels of ADC can be eight channels of line-in from IOB [7:0] or one channel microphone (MIC) input through amplifier PGA controller, and AGC controller. The MIC amplifier circuit is capable of reducing common mode noise by transmitting signals through differential MIC Inputs (MICN, MICP). Moreover, an external resistor can be applied to adjust microphone gain and operating time of AGC.

7.13 USB Device Function (by body)

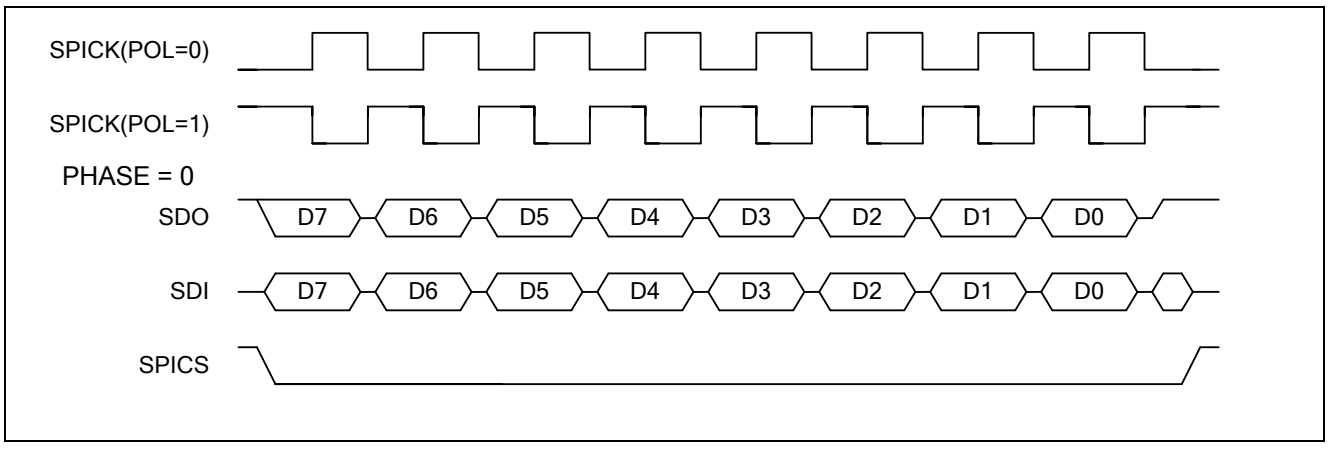
Some of the GPCE4xxxx series provide device function which is compatible with USB 2.0 full-speed standard. An USB transceiver is also built-in.

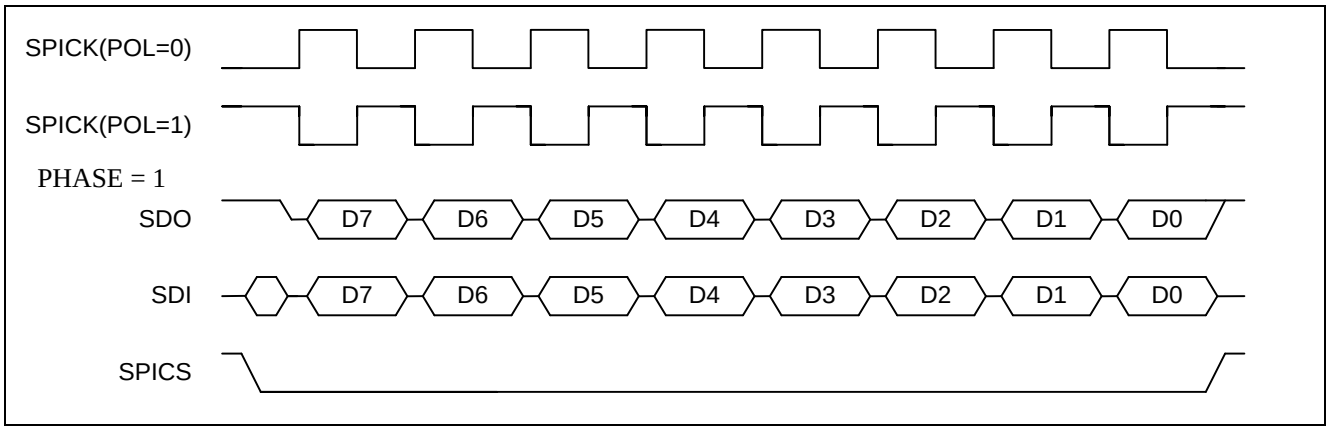
7.14 SPIFC

A Serial Peripheral Interface flash controller (SPIFC) is featured to facilitate communication between GPCE4xxxx with other devices and components, especially for SPI FLASH. The SPIFC supports one- I/O, two-I/O, four-I/O mode of SPI flash. The SPIFC also supports auto mode which can access SPI flash data directly, therefore user's program can be placed at external SPI flash. There are six control signals on SPI - SPICS (IOA12), SPICK (IOA13), SDI (IOA14), SDO (IOA15), SPIIO3 (IOA10, only for 4 I/O mode), and SPIIO2 (IOA11, only for 4 I/O mode).

7.14.1 SPI2

A Serial Peripheral Interface controller (SPI2) is built in GPCE4xxxx to facilitate communicating with other devices and components. There are four control signals on SPI2 - SPICS (IOB12), SPICK (IOB13), SDI (IOB14), and SDO (IOB15).





7.15 Audio output

Two sets of 16-bit software channel with noise filter is supported. There is one 14-bit DAC with push-pull amplifier for direct audio output which can mix the analog input signal (ACIN) and the two software channels.

8 ELECTRICAL SPECIFICATIONS

8.1 Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 4.0V
PortA/B/C Pad Supply Voltage	V_{IO}	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see DC Electrical Characteristics.

8.2 DC Characteristics (VDD_REG = 3.3V, VDDIO = 4.5V (IOA & IOB & IOC), TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD_REG	2.4	-	5.5	V	-
Operating Current	I_{OP}	-	23	29	mA	F_{OSC} = 48MHz, AD, DAC disable, no load
Standby Current	I_{STB}	-	-	10	μA	Disable 32KHz crystal
				15	μA	Enable 32KHz,Disable PLL(F_{OSC})
Input High Level	V_{IH}	0.7VDD_IO	-	VDD_IO	V	-
Input Low Level	V_{IL}	0	-	0.3VDD_IO	V	-
Output High Current (IOA[9:0], IOB, IOC)	I_{OH}	7	14	21	mA	V_{OH} = 0.7VDD_IO
Output High Current (IOA[15:10])	I_{OH}	14	27	41	mA	V_{OH} = 0.7VDD_IO
Output Low Current (IOA[9:4], IOB, IOC)	I_{OL}	13	23	36	mA	V_{OL} = 0.3VDD_IO
Output Low Current (IOA[3:0])	I_{OL}	22	44	66	mA	V_{OL} = 0.3VDD_IO
Output Low Current (IOA[15:10])	I_{OL}	7	13	20	mA	V_{OL} = 0.3VDD_IO, high drive disable
Output Low Current (IOA[15:10])	I_{OL}	13	25	37	mA	V_{OL} = 0.3VDD_IO, high drive enable
Input Pull-Low Resister (IOA, IOB, IOC)	R_{PL}	80	120	160	KΩ	V_{IN} = VDD_IO
Input Pull-High Resister (IOA, IOB, IOC)	R_{PH}	80	120	160	KΩ	V_{IN} = VSS_IO
Internal ROSC frequency deviation	⊿F/F	-3%	32768	+3%	HZ	V33_REG = 3.3V
Internal 6M ROSC frequency deviation	⊿F/F	-3%	6000000	+3%	HZ	V33_REG = 3.3V

8.3 DC Characteristics (VDD_REG = 3.3V, VDDIO = 3.3V (IOA & IOB & IOC), TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD_REG	2.4	-	5.5	V	-
Operating Current	I_{OP}	-	23	29	mA	F_{OSC} = 48MHz, AD, DAC disable, no load

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Standby Current	I_{STB}	-	-	10	μA	Disable 32KHz crystal
				15	μA	Enable 32KHz,Disable PLL(F_{OSC})
Input High Level	V_{IH}	0.7VDD_IO	-	VDD_IO	V	-
Input Low Level	V_{IL}	-	-	0.3VDD_IO	V	-
Output High Current (IOA[9:0], IOB, IOC)	I_{OH}	4	8	12	mA	V_{OH} = 0.7VDD_IO
Output High Current (IOA[15:10])	I_{OH}	8	15	22	mA	V_{OH} = 0.7VDD_IO
Output Low Current (IOA[9:4], IOB, IOC)	I_{OL}	7	14	21	mA	V_{OL} = 0.3VDD_IO
Output Low Current (IOA[3:0])	I_{OL}	13	26	39	mA	V_{OL} = 0.3VDD_IO
Output Low Current (IOA[15:10])	I_{OL}	4	7	10	mA	V_{OL} = 0.3VDD_IO, high drive disable
Output Low Current (IOA[15:10])	I_{OL}	7	14	21	mA	V_{OL} = 0.3VDD_IO, high drive enable
Input Pull-Low Resister (IOA, IOB, IOC)	R_{PL}	80	120	160	KΩ	V_{IN} = VDD_IO
Input Pull-High Resister (IOA, IOB, IOC)	R_{PH}	80	120	160	KΩ	V_{IN} = VSS_IO
Internal ROSC frequency deviation	⊿F/F	-3%	32768	+3%	HZ	V33_REG = 3.3V
Internal 6M ROSC frequency deviation	⊿F/F	-3%	6000000	+3%	HZ	V33_REG = 3.3V

8.4 ADC Characteristics (V33_ADC = 3.3V, TA = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
ADC LINE_IN Input Voltage Range from IOB[7:0]	VINL (Note 1)	VSS-0.3	-	V33_ADC+0.3	V
ADC Microphone Input Voltage Range	VINM	VSS-0.3	-	V33_ADC+0.3	V
Resolution of ADC	RESO	-	-	12	bits
Signal-to-Noise Plus Distortion of ADC from Line in	SINAD (Note 3)	-	50	-	dB
Effective Number of Bit	ENOB (Note 4)	7.0	8.0	-	bits
Integral Non-Linearity of ADC	INL	-	±5.0	-	LSB (Note 2)
Differential Non-Linearity of ADC	DNL (Note 6)	-	±1.0	-	LSB
AD Conversion Rate	F_{CONV}	-	-	F_{CPU}/256	Hz
Microphone Amplifier Gain	A_{MIC}	-	-	42(Note 5)	dB

Note1: Internal protection diodes clamp the analog input to V33_ADC and VSS. These diodes allow the analog input to swing from (VSS-0.3V) to (V33_ADC+0.3V) without causing damage to the devices.

Note2: LSB means Least Significant Bit. With VINL = 2.6V, 1LSB = 2.6V/2^12 = 0.635mV.

Note3: The SINAD testing condition at VINLp-p = 0.8*V33_ADC, F_{CONV} = Fcpu/512 = 49MHz/256 = 192KHz, Fin=1.0KHz Sine waves at V33_ADC = 3.0V from the IOB [7:0] input.

Note4: ENOB = (SINAD-1.76)/6.02.

Note5: The microphone amplifier maximum gain = 15 * (60K/(1.5K+REXT) V/V. The REXT is external resistor between OPI and MICOUT. The gain is 132V/V (=42dB) when REXT is 5.1K.

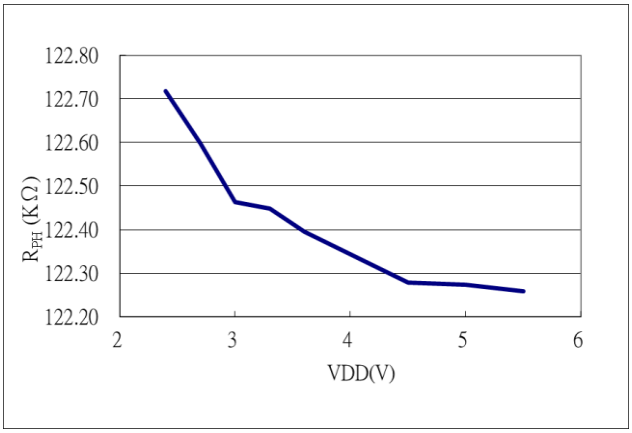
8.5 DAC Characteristics (VDD_DAC = 5.0V, TA = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
DAC Resolution	RESO	-	-	16	bit
THD+n (5V @0.6W)	-	-	1	-	%
Noise at No Signal	-	-	-87	-	dBr A
Dynamic Range(-60dB)	-	-	-86	-	dBr A

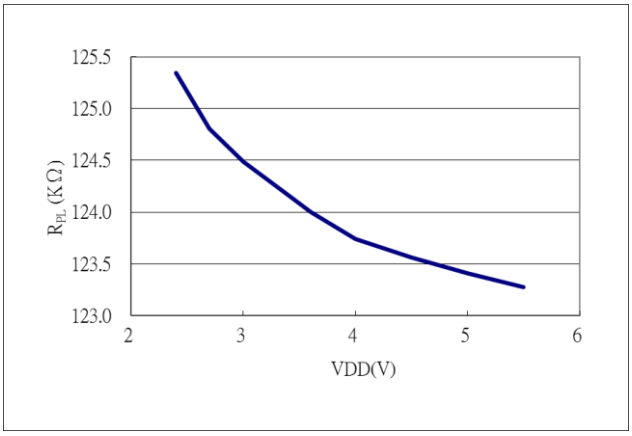
8.6 Regulator Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage	VREGI	2.4	-	5.5	V	
Maximum Current Output	IREGO	-	-	60	mA	VDD_REG (Regulator in)= 4.5V, △VDD (Regulator out) <100mV
Output Voltage	VREGO	2.4	3.3	3.3	V	
Standby Current	IRGES	-	5	-	uA	

8.7 Pull High Resistance and VDD(VDD_IO)

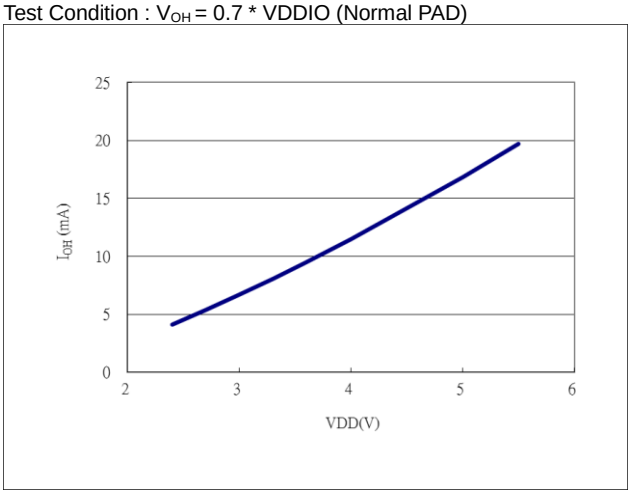


8.8 Pull Low Resistance and VDD(VDD_IO)



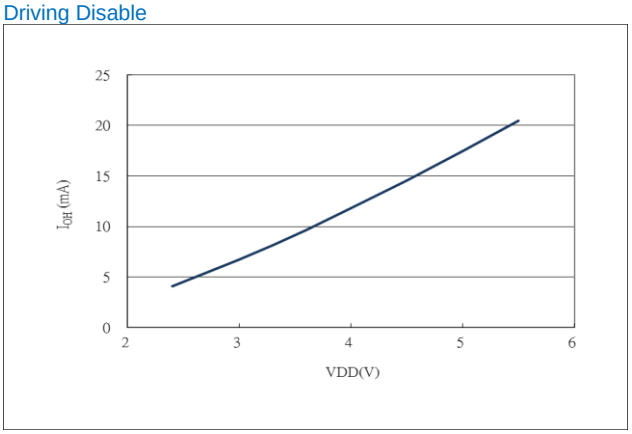
8.9 IO Output High Current and VDD(VDD_IO)

Test Condition : V_{OH} = 0.7 * VDDIO (Normal PAD)



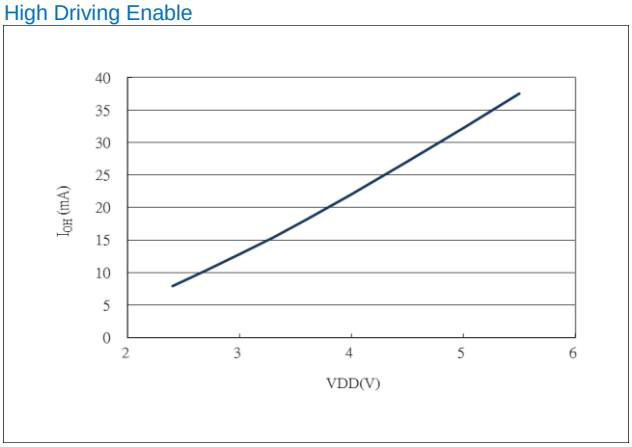
8.10 IO Output High Current and VDD(VDD_IO)

Test Condition: V_{OH} = 0.7 * VDDIO (SPI PAD – IOA [15:10]) High Driving Disable



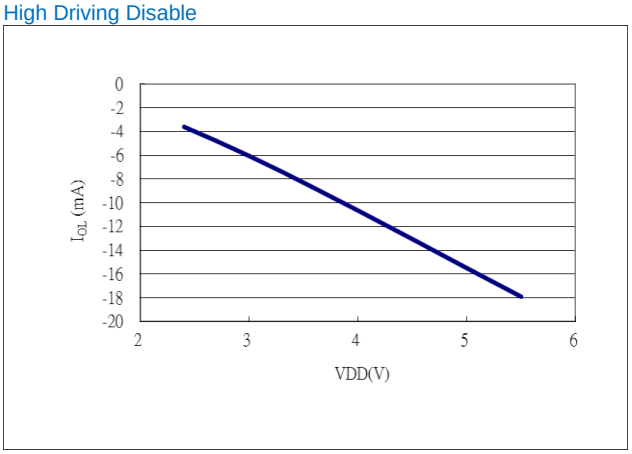
Test Condition : V_{OH} = 0.7 * VDDIO (SPI PAD – IOA [15:10])

High Driving Enable



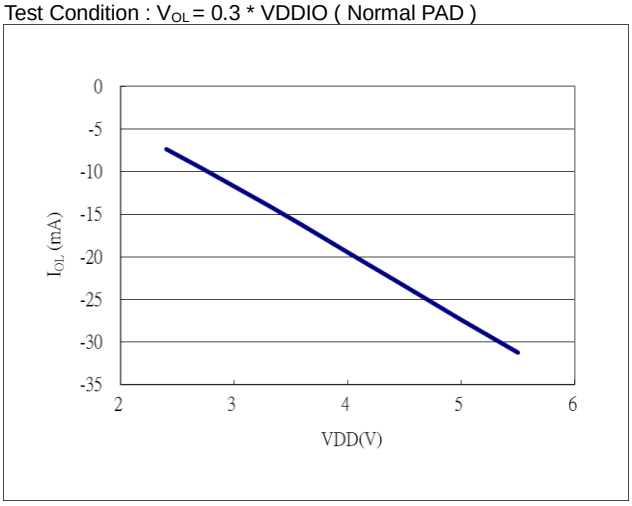
Test Condition : V_{OL} = 0.3 * VDDIO (SPI PAD – IOA [15:10])

High Driving Disable



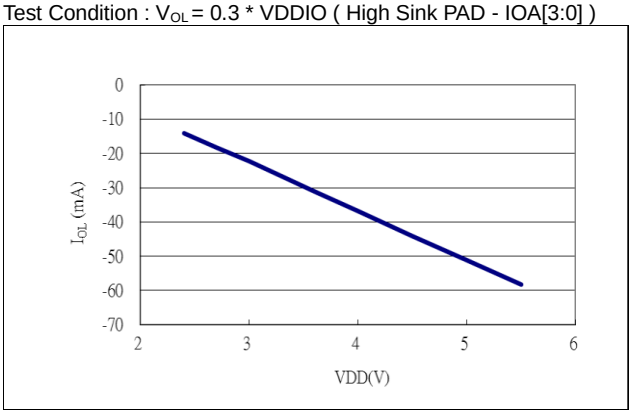
8.11 IO Output Low Current and VDD(VDD_IO)

Test Condition : V_{OL} = 0.3 * VDDIO (Normal PAD)



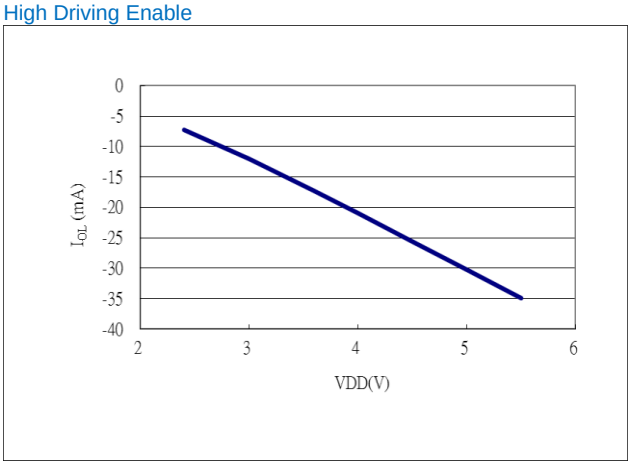
8.12 IO Output Low Current and VDD(VDD_IO)

Test Condition : V_{OL} = 0.3 * VDDIO (High Sink PAD - IOA[3:0])

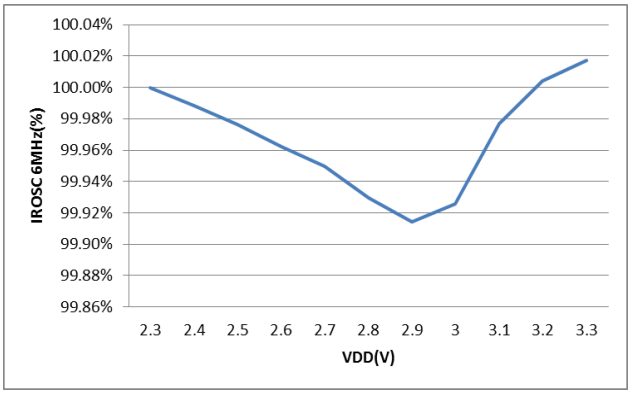


Test Condition : V_{OL} = 0.3 * VDDIO (SPI PAD – IOA [15:10])

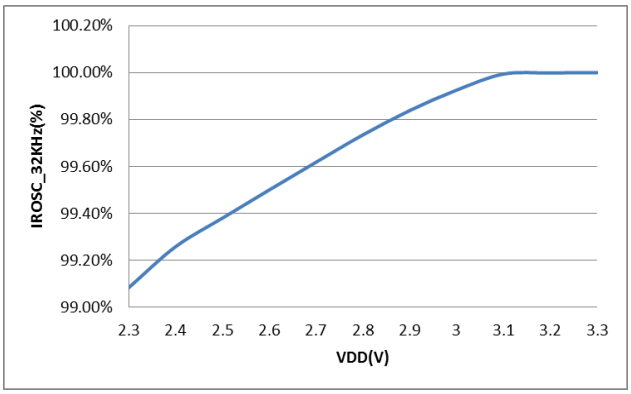
High Driving Enable



8.13 Internal ROSC 6M and VDD(VDD_IO)

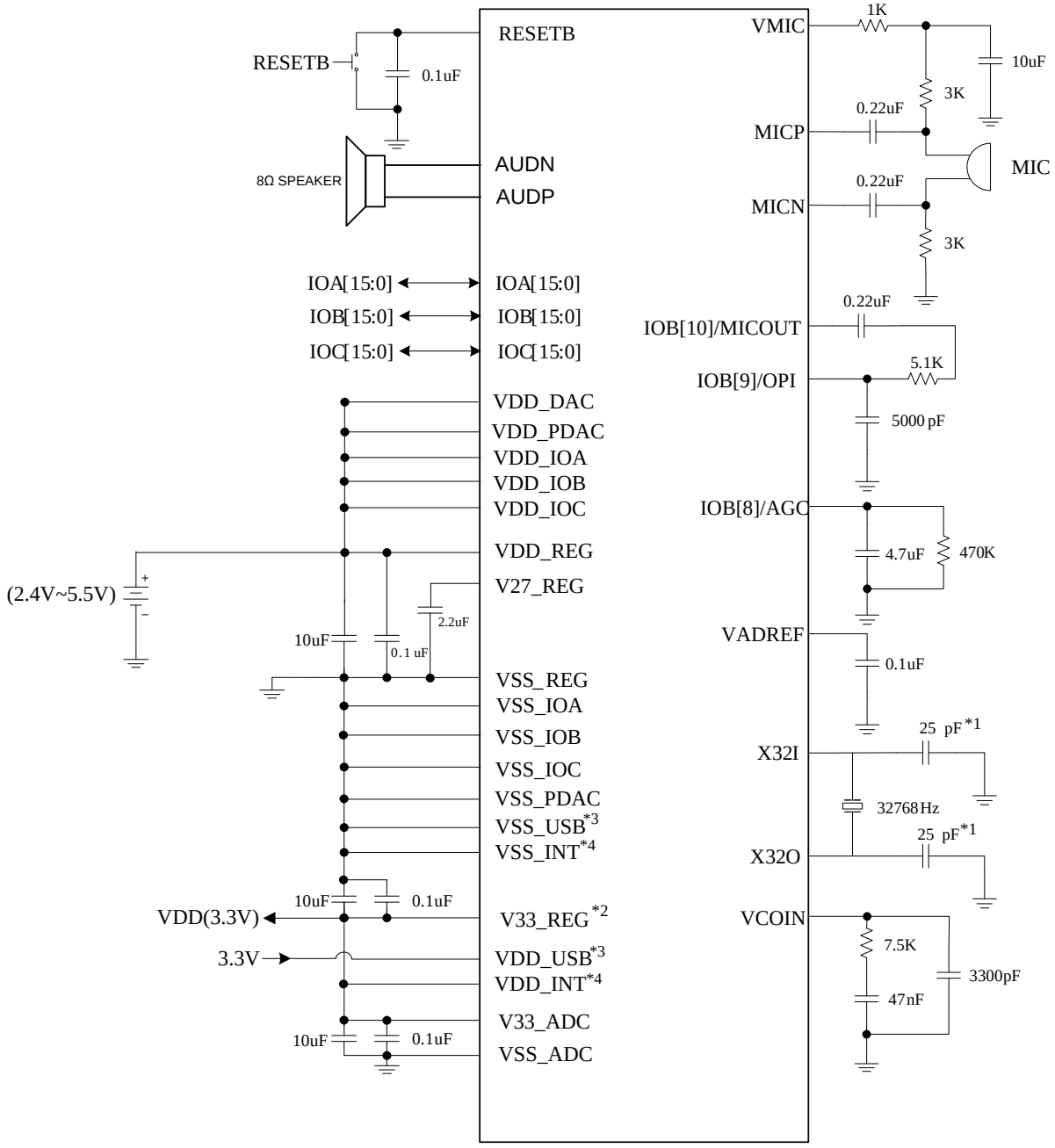


8.14 Internal ROSC 32K and VDD(VDD_IO)



9 APPLICATION CIRCUITS

9.1 Application Circuit with Regulator, PLL6M and XTAL32K Selected



Application Circuit(MIC_IN)

.

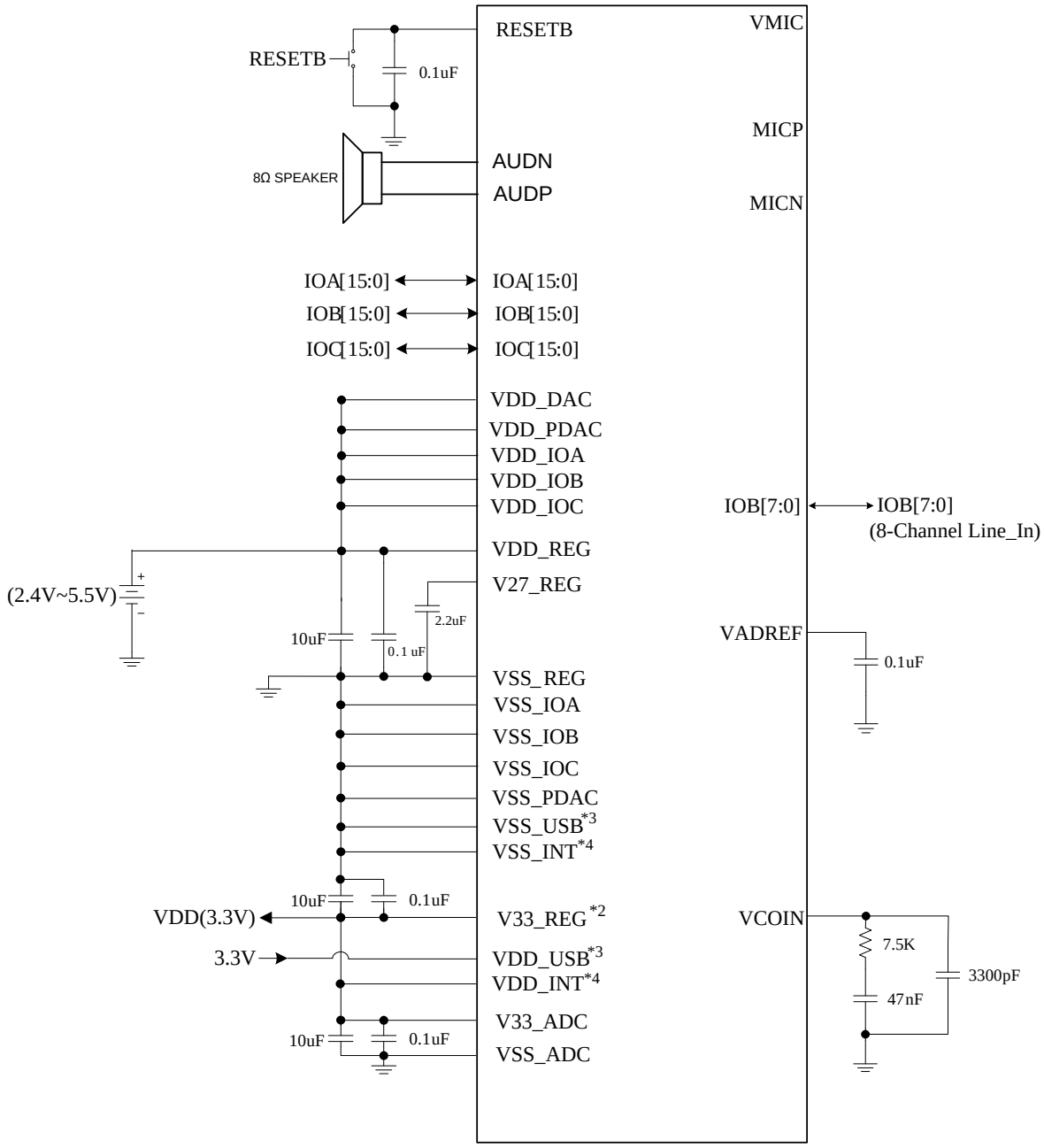
Note1: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~60K and CL1=CL2 =26~36pF (including PCB parasitic loading; for example, user should apply additional 20~30pF on X32I and X32O if PCB parasitic loading is 6pF)

Note2: V33_REG is output of built-in regulator with maximum current 60mA. It is recommended that only use it for internal power pad.

Note3: VSS_USB and VDD_USB are supported by body (ref. to "6 SIGNAL DESCRIPTIONS"). It is recommended that the supplied power of VDD_USB uses external power instead of V33_REG.

Note4: VSS_INT and VDD_INT are supported by body (ref. to "6 SIGNAL DESCRIPTIONS").

9.2 Application Circuit with Regulator, PLL6M and ROSC32K Selected



Application Circuit(LINE_IN)

.

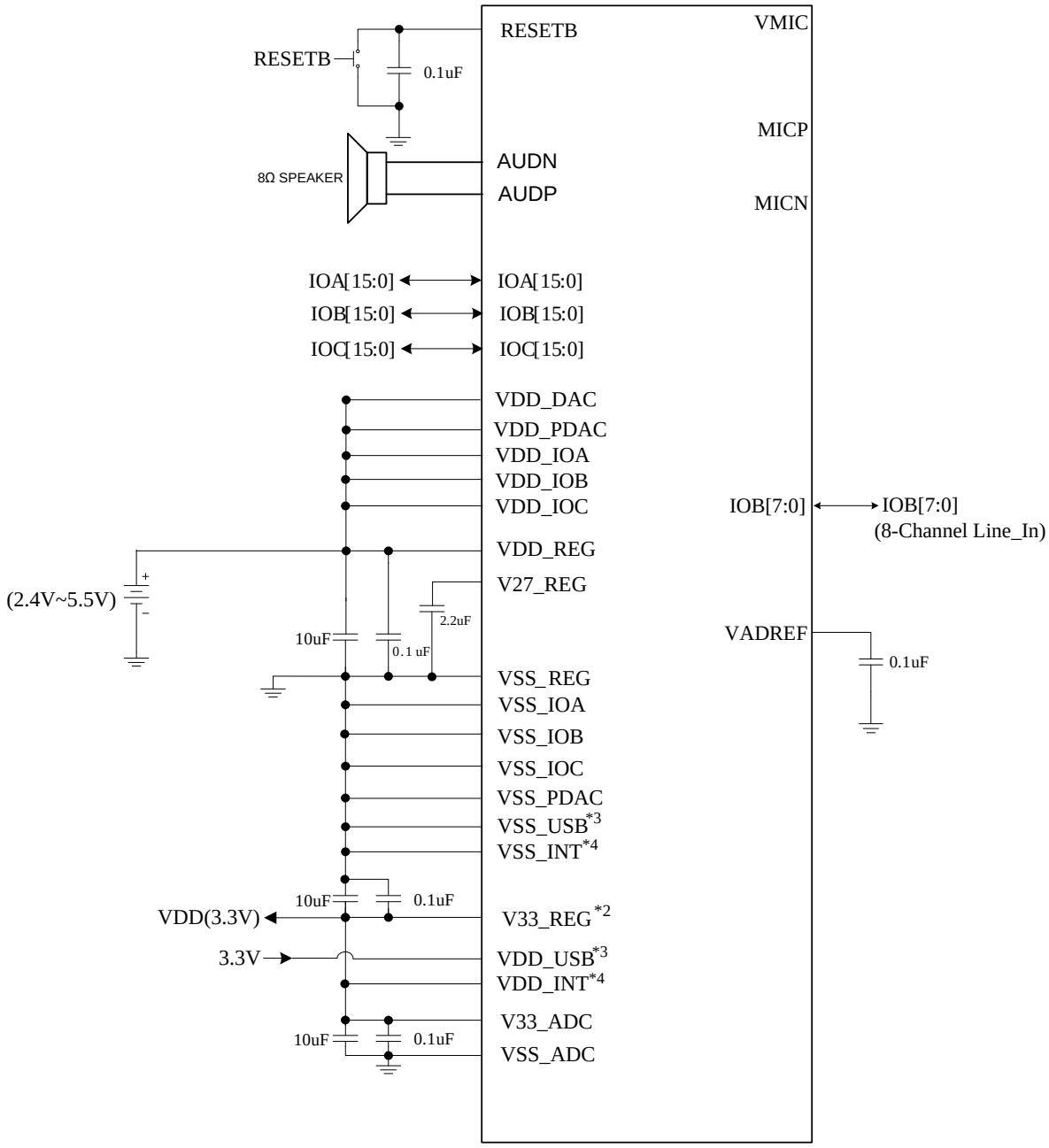
Note1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note2: V33_REG is output of built-in regulator with maximum current 60mA. It is recommended that only use it for internal power pad.

Note3: VSS_USB and VDD_USB are supported by body (ref. to "6 SIGNAL DESCRIPTIONS"). It is recommended that the supplied power of VDD_USB uses external power instead of V33_REG.

Note4: VSS_INT and VDD_INT are supported by body (ref. to "6 SIGNAL DESCRIPTIONS").

9.3 Application Circuit with Regulator, ROSC6M and ROSC32K Selected



Application Circuit(LINE_IN)

.

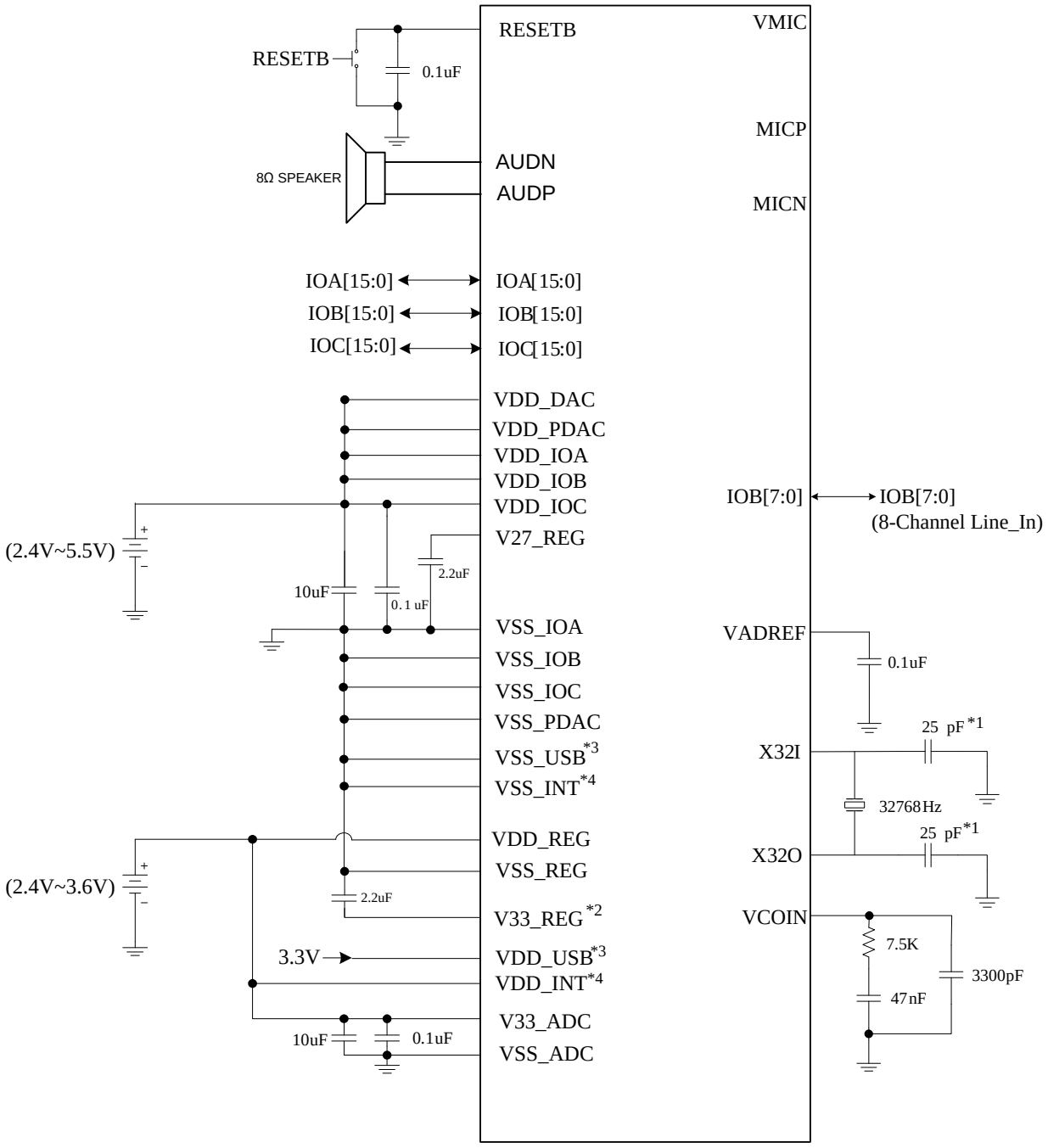
Note1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note2: V33_REG is output of built-in regulator with maximum current 60mA. It is recommended that only use it for internal power pad.

Note3: VSS_USB and VDD_USB are supported by body (ref. to "6 SIGNAL DESCRIPTIONS"). It is recommended that the supplied power of VDD_USB uses external power instead of V33_REG.

Note4: VSS_INT and VDD_INT are supported by body (ref. to "6 SIGNAL DESCRIPTIONS").

9.4 Application Circuit without Regulator, PLL6M and XTAL32K Selected



Application Circuit(LINE_IN)

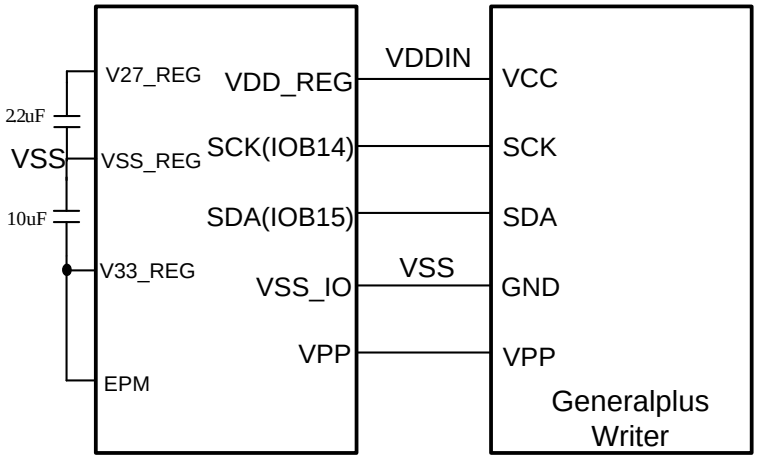
Note1: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~60K and CL1=CL2 =26~36pF (including PCB parasitic loading, for example, user should apply additional 20~30pF on X32I and X32O if PCB parasitic loading is 6pF).

Note2: V33_REG is output of built-in regulator with maximum current 60mA. It is recommended that only use it for internal power pad.

Note3: VSS_USB and VDD_USB are supported by body (ref. to “6 SIGNAL DESCRIPTIONS”). It is recommended that the supplied power of VDD_USB uses external power instead of V33_REG.

Note4: VSS_INT and VDD_INT are supported by body (ref. to “6 SIGNAL DESCRIPTIONS”).

9.5 OTP ROM Programming Circuit (by body)



Note: There must be 3V or 5V power connected to VDD_IOB, VSS_IOB should be connected to ground.

10 PACKAGE/PAD LOCATIONS

10.1 Ordering Information

Body	Product Number	Package Type
GPCE4P096UA	GPCE4P096UA-NnnV-C	Chip form
	GPCE4P096UA-NnnV-QL09x	Green Package – LQFP128
	GPCE4P096UA-NnnV-QL03x	Green Package – LQFP80
	GPCE4P096UA-NnnV-QL02x	Green Package – LQFP64
	GPCE4P096UA-NnnV-QV09x	Green Package – QFN64
	GPCE4P096UA-NnnV-QL23x	Green Package – LQFP48
GPCE4096UA	GPCE4096UA-NnnV-C	Chip form
	GPCE4096UA-NnnV-QL09x	Green Package – LQFP128
	GPCE4096UA-NnnV-QL03x	Green Package – LQFP80
	GPCE4096UA-NnnV-QL02x	Green Package – LQFP64
	GPCE4096UA-NnnV-QV09x	Green Package – QFN64
	GPCE4096UA-NnnV-QL23x	Green Package – LQFP48
GPCE4096A	GPCE4096A-NnnV-C	Chip form
	GPCE4096A-NnnV-QL09x	Green Package – LQFP128
	GPCE4096A-NnnV-QL03x	Green Package – LQFP80
	GPCE4096A-NnnV-QL02x	Green Package – LQFP64
	GPCE4096A-NnnV-QV09x	Green Package – QFN64
	GPCE4096A-NnnV-QL23x	Green Package – LQFP48
GPCE4064A	GPCE4064A-NnnV-C	Chip form
	GPCE4064A-NnnV-QL09x	Green Package – LQFP128
	GPCE4064A-NnnV-QL03x	Green Package – LQFP80
	GPCE4064A-NnnV-QL02x	Green Package – LQFP64
	GPCE4064A-NnnV-QV09x	Green Package – QFN64
	GPCE4064A-NnnV-QL23x	Green Package – LQFP48

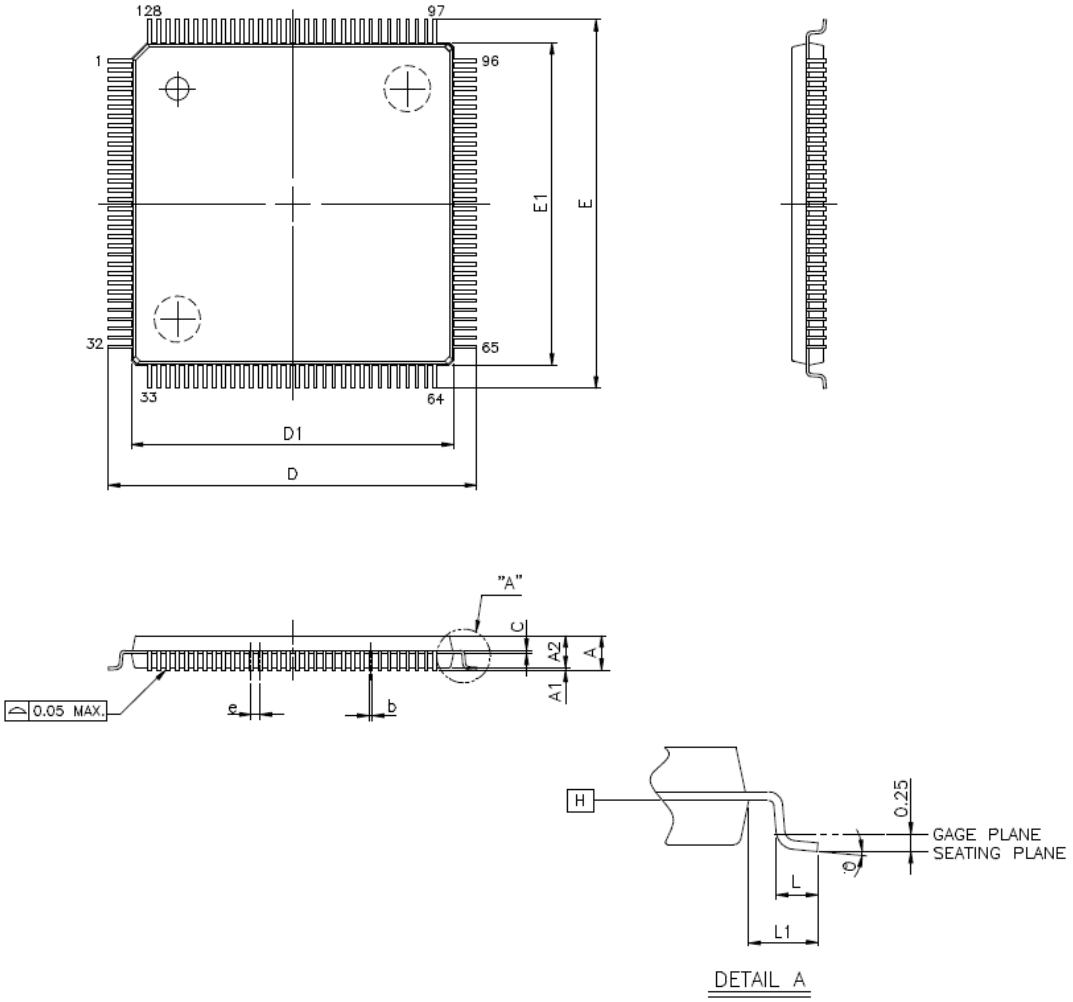
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

10.2 Package Information

10.2.1 LQFP 128L Outline Dimensions

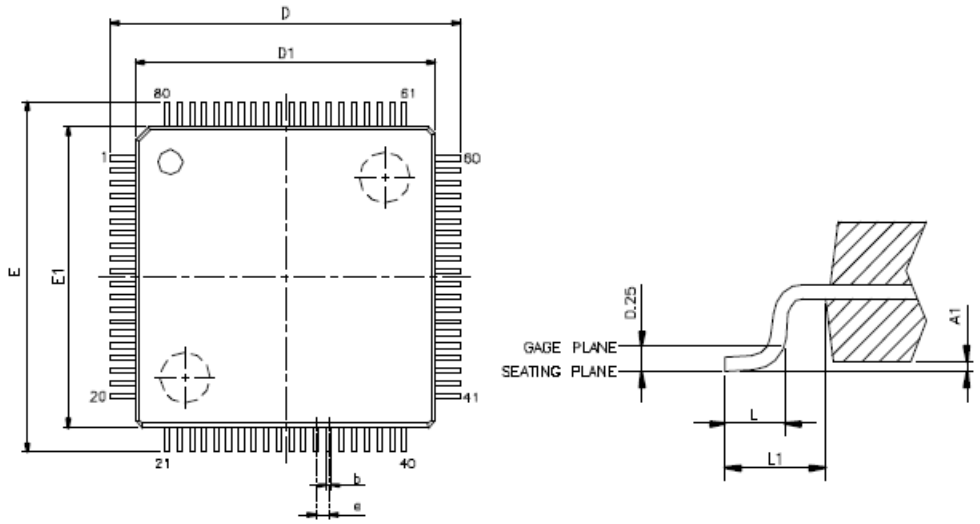


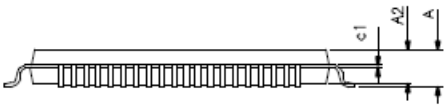
Symbols	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
⚠1 b	0.13	0.16	0.23
c	0.09	-	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Notes:

1. Datum plane H is located at the bottom of the mold parting line coincident with where the lead exits the body.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane H.
3. Dimension b does not include dambar protrusion.

10.2.2 LQFP 80 Outline Dimensions





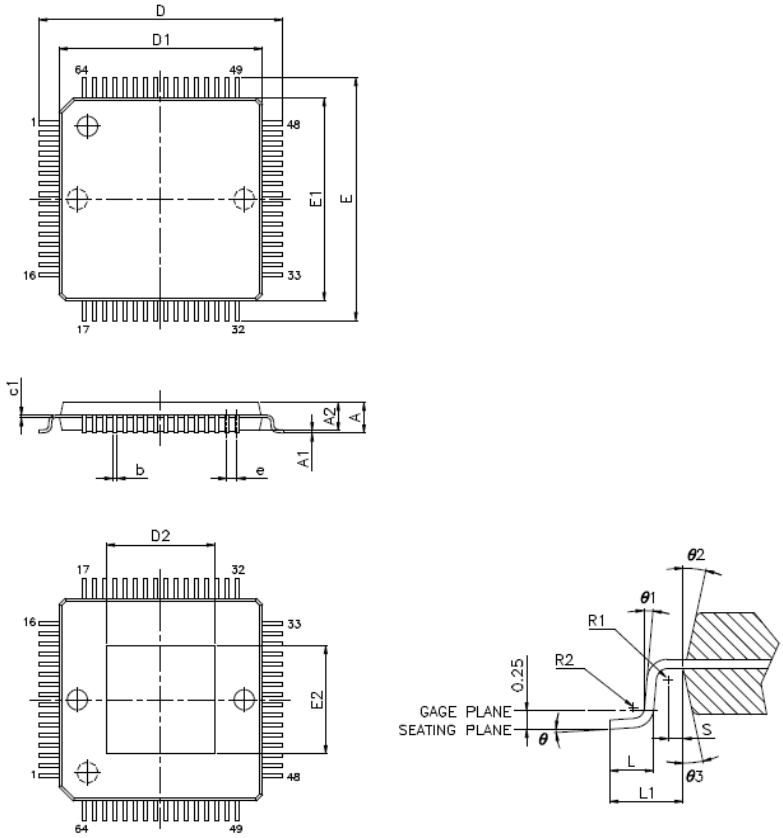
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	12 BSC	
D1	10 BSC	
E	12 BSC	
E1	10 BSC	
e	0.4 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:

1. JEDEC OUTLINE:MS-026 BCE
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

10.2.3 LQFP 64 Outline Dimensions



(THERMALLY ENHANCED VARIATIONS ONLY)

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c1	0.09	—	0.16
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20 REF		
θ	3.5° REF		
θ1	5.0° REF		
θ2	12° REF		
θ3	12° REF		
R1	0.16 REF		
R2	0.15 REF		

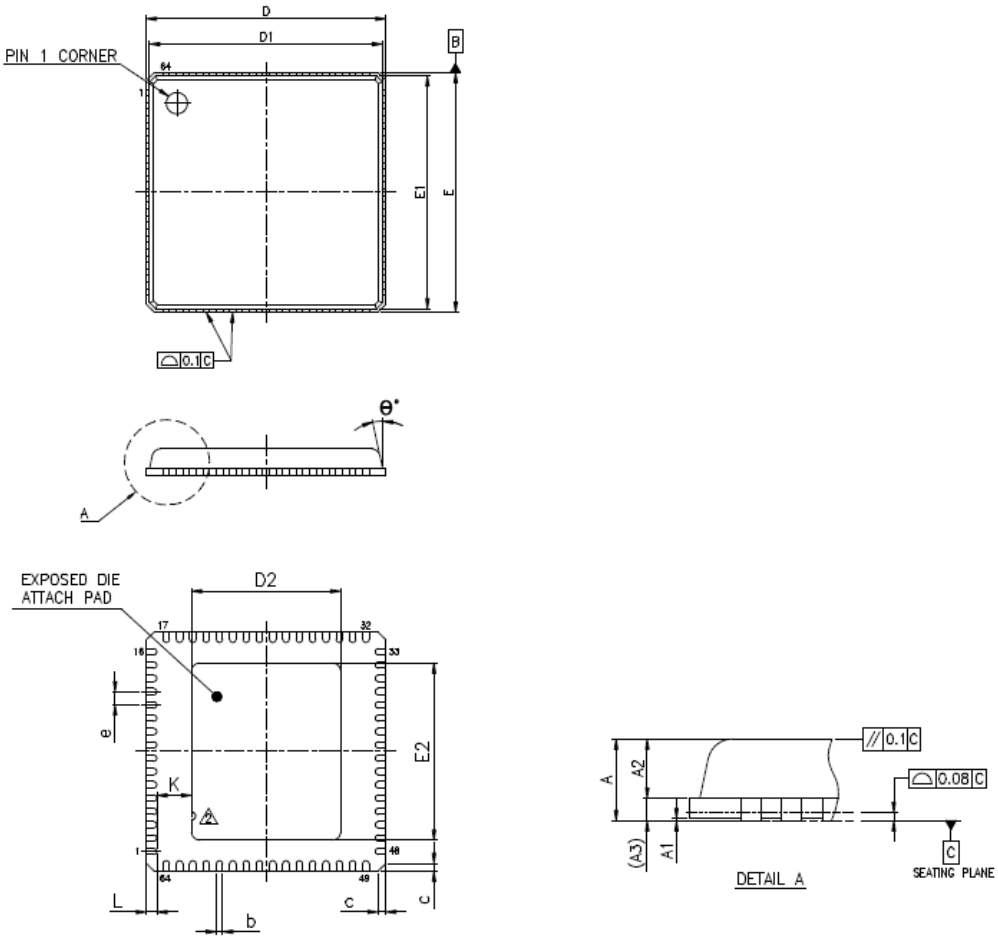
⚠5 THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D2	
	MIN.	MAX.	MIN.	MAX.
210X21E	4.27	5.33	4.27	5.33
260X26E	5.28	6.60	5.28	6.60

NOTES:

1. JEDEC OUTLINE :
   MS-026 BCD
   MS-026 BCD-HD(THERMALLY ENHANCED VARIATIONS ONLY)
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

10.2.4 QFN 64 Outline Dimensions



⚠ PIN1位置辨識由斜角改為半圓孔.

SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.20 REF.	
b	0.18	0.25	0.30
c	0.24	0.42	0.60
D	8.90	9.00	9.10
D1	8.65	8.75	8.85
E	8.90	9.00	9.10
E1	8.65	8.75	8.85
e		0.50 BSC.	
K	0.20	—	—
L	0.30	0.40	0.50
θ°	0.00	—	12.00

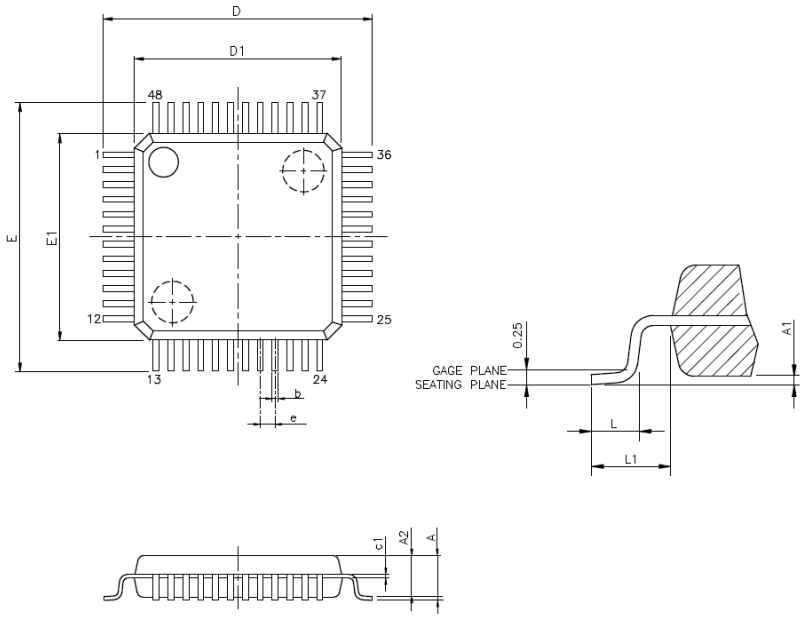
UNIT : mm

⚠	EXPOSED PAD			
	D2		E2	
DIE PAD	MIN.	MAX.	MIN.	MAX.
190X230MIL	4.40	5.20	5.45	6.25
230X230MIL	5.30	5.60	5.30	5.60

UNIT : mm

NOTES :
1. JEDEC : N/A.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION "b" APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. THE PIN #1 IDENTIFIER EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. DIMENSION "A1" APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

10.2.5 LQFP 48 Outline Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:

1. JEDEC OUTLINE:MS-026 BBC
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

11 DISCLAIMER

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12 REVISION HISTORY

Date	Revision #	Description	Page
Jun. 26, 2017	1.1	Add package LQFP48 at 6.1.6, 6.2.6, 6.3.6, 10.1 and 10.2.5.	13,20,27, 42,47
Apr. 17, 2017	1.0	Original	45