GPCE4 Series Confirmation Sheet

V1.6 01/13/2017

Customer		**Date**	
Project Title		**Code No.**	
Project Description			
Body Type	☐ GPCE4P096UA (46K-word OTP) ☐ GPCE4096UA (46K-word ROM) ☐ GPCE4096A (46K-word ROM) ☐ GPCE4064A (32K-word ROM) ☐ GPCE4P096UA_0001 (46K-word OTP) ☐ GPCE4096UA_0001 (46K-word ROM) ☐ GPCE4096A_0001 (46K-word ROM) ☐ GPCE4064A_0001 (32K-word ROM)	**Packaging Type**	☐ Chip-form ☐ Package
PLL Source - **6MHz and 48MHz**	☐ Crystal 32768Hz + PLL 6M ☐ Internal ROSC32K + Internal ROSC6M	**CPU Freq (MHz):** ☐6MHz ☐12MHz ☐18MHz ☐24MHz ☐30MHz ☐36MHz ☐42MHz ☐48MHz **Wait State Cycle:** ☐2-cycle ☐3-cycle or above Note: The 2-cycle option does not support 32MHz or above (CPU Clock)	
Working Voltage (VDD)	☐ 2.4V ~ 5.5V		
I/O Voltage (VDDIO)	☐ 2.4V ~ 5.5V		
Regulator Output Option	☐ 3.3V ☐ 3.0V ☐ 2.8V		
Watchdog	☐ Enable ☐ Disable		
Security Option	☐ Enable ☐ Disable (For OTP only)		
Program Unique ID	☐ Yes ☐ No (Example: BLE Mac Address, …)		

Release code file (fill "00H" for unused area)

Binary filename (*.tsk):	**Binary file check sum:**

SRAM:

GPCE4P096UA/4096UA/4096A/4064A/4P096UA_0001/4096UA_0001/4096A_0001/4064A_001: 4K words + 2K words cache memory ($0000 ~ $0FFF) ☐Check

GPCE4P096UA/4096UA/4096A/4064A/4P096UA_0001/4096UA_0001/4096A_0001/4064A_001: 6K words without cache memory ($0000 ~ $17FF) ☐Check

ROM:

GPCE4P096UA/4096UA/4096A/4P096UA_0001/4096UA_0001/4096A_0001: 46K words ($4800 ~ $FFFF)

GPCE4064A/4064A_0001: 32K words ($4800 ~ $C7FF) ☐Check

Input / Output

IOA Port

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Input																
Output																
Wakeup Key Input																

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IOB Port

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Input																
Output																
Wakeup Key Input																
A/D Line - In Input																

IOC Port

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Input																
Output																
Wakeup Key Input																

Hardware / Software

- If ADC Line_in is used, please check the Line_In input (shared with IOB0~7) voltage range: 0 V ~ AVDD
- If ADC Mic_in is used, Note that IOB8~11 are shared IO pins with MIC circuit.
- If Serial Peripheral Interface (SPI1/SPI2) is used, please check the following:
  a. While in standby mode, users must ensure that SPI interface is not under floating condition in order to make standby current stabilized. For more information, please refer to AN0088 application note.
  b. For SPI1 Share IO, the Driving and Sink capability on IOA10~IOA15 are the same.
  c. After SPI1 DMA Starts, wait at least 8 CPU clocks before checking DMA Busy Flag.
- If watchdog is enabled, watchdog port ($3034H) must be cleared within 0.875 seconds by writing 0x5555. Please refer to datasheet for more detailed information.
- If sleep mode is applied, please check the following:
  a. Make sure 32768Hz must be enabled or disabled during sleep mode.
- No floating state is allowed on I/O if used for key wakeup. All GPIOs (IOA/B/C) feature wakeup function. We suggest masking the unused pins if possible.
- Make sure the release code (*.tsk) is generated by unSP IDE debug mode.
- In using GPCE4 series, VDD_REG must be connected with Power_in and V33_REG must be connected with a 10uF to GND.
- In using GPCE4 series, V27_REG must be connected with a 2.2uF to GND.
- P_System_Clock's bit [7:5] cannot be 111B.
- To disable cache, extra five NOPs are required to avoid unexpected operations on Pipe Line.
- The data port on GPIO is read-only.
- The stereo mode on DAC does not support Gain = 0.

☐ **Check-by ticking off this box, customer understands that the above conditions are fully met and verified.**

General programming checklist

The general programming checklist intends to provide some general characteristics about GENERALPLUS devices. It is the customer's responsibility to check all the information in the list. No responsibility is assumed by GENERALPLUS for any non-checked box even this confirmation sheet has been approved by GENERALPLUS. Make sure the following conditions are met and verified:

- All used SRAM must be initialized after power on (Strongly recommended).
- Make sure the used SRAM variables are not over stack reserved area.
- Make sure the Interrupt section is located in the page0 or is declared as .TEXT section ($4800-$FFFF).
- Make sure no current leakage in I/O or speaker amplifier during sleeping.
- Make sure all I/Os are not floating during sleeping.
- If IO is a wakeup source, I/O data & attribute ports must be latched before entering into sleep mode.
  Example:

```
R1 = [P_IOC_Attrib];
R1 = [P_IOC_Data];      // Latch IOC
```


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- Non-used I/O ports must be masked off (for input process).

  Example, if IOA[0:7] are input: R1 = [P_IOA_Data]; ; Read I/O port A Data

  R1 & = 0x00FF; ; Mask higher byte

  CMP R1,0x0011; ; Lower byte is available for compare operation

- For those IOs don't need wakeup function, make sure the corresponding bits in P_IOx_WakeUp_Mask are set to "1".

  Example: Suppose IOC does not need wakeup function, please do the following:

  R1 = 0xFFFF;

  [P_IOC_WakeUp_Mask] = R1;

☐**Check-by ticking off this box, customer understands that the above conditions are fully met and verified.**

Document version

To ensure the correct version of document is used, please fill out the followings:

(A). GPCE4 Series Programming Guide Version_____

(B). μ'nSP™ Programming Tools User's Manual Version_____

(C). μ'nSP™ Assembly Programming Guide Version_____

(D).Other documents (if any)_____

Development tool / Board version

To ensure the correct version of hardware is used, please fill out the followings:

(A).Emulation Board Version_____

(B).Emulation Chip Version_____

(C).Piggyback Version(if used) _____

(D).Others (if any)_____

To ensure the correct version of software is used, please fill out the following:

(A). μ'nSP™ IDE Version_____

(B).SACM Library Version(if used)_____

☐S200 ☐S480/720 ☐S530 ☐A1600 ☐A1601 ☐A1800 ☐A3400Pro ☐A3600 ☐DVR520 ☐DVR1600
☐DVR1800 ☐DVR3200 ☐DVR4800 ☐MS01 ☐MS02

(C).Others (if any)_____

For Third Party Application

Cyberon voice recognition solution is applied in this code ☐Yes ☐No

If yes, please fill out the followings:

(A). Types of solutions: ☐SI only ☐SD only ☐SID(both SI & SD) ☐SV ☐PSI

(B). Modeling Toolkit IDE Version_____

(C). Library Version: BSRV_____.lib

(D). SDK Programming Guide Version _____

(E). Others (if any)_____

Customer note	GENERALPLUS note
Signature: _____	**Signature:** _____

Note: Please send/fax this form to GENERALPLUS. GENERALPLUS will return it back with signature.

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