DATA SHEET

GPMD5130A

5V Full Bridge Driver for High Integration, High Efficiency and Low Cost Wireless

DEC. 23, 2015

Version 1.0

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1A Ultra-Low Dropout Linear Regulator

1. GENERAL DESCRIPTION

GPMD5130A is a highly integrated 5V full bridge power IC optimized for wireless power transmitter solution. It is works with a transmitter controller to create a low cost and high performance wireless power transmitter compliant with WPC 1.2 or for any custom transmitter solutions. The device integrates all critical functions, such as high efficiency power FETs, low EMI FET driver, boost strap circuit, 2.5V LDO and current measurement. The proprietary current measurement circuit provides accurate current reading for FOD (Foreign Object Detection) power measurement and pulse-by-pulse signal for in-band communication. It eliminates the current sense resistor and amplifier circuit, and thus saves cost and power losses.

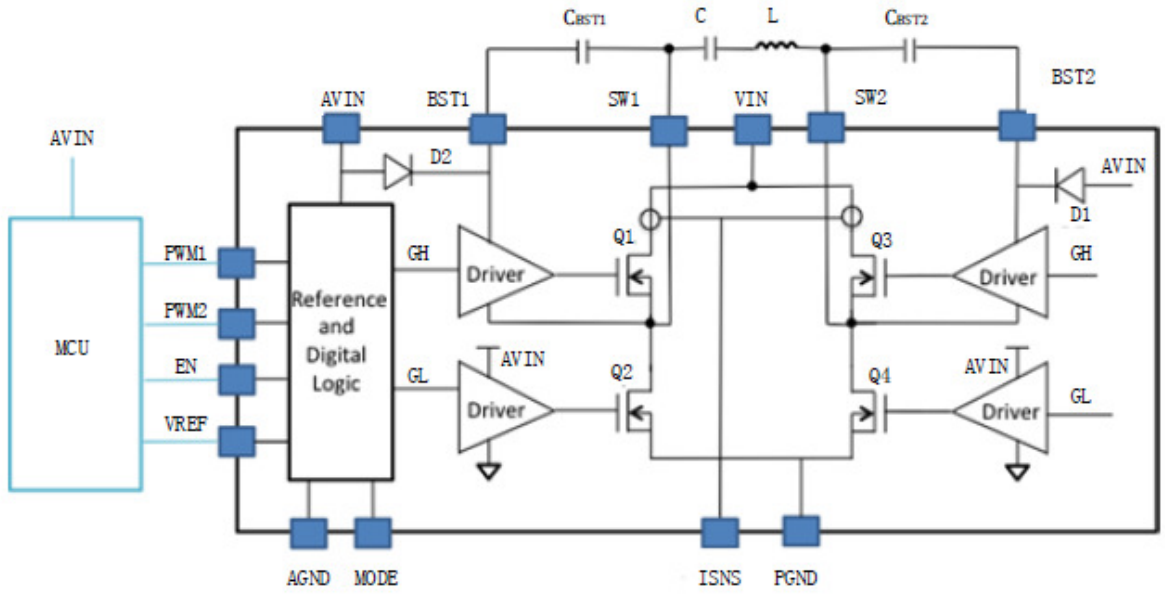
The IC also includes protection functions such as input under-voltage lockout, short circuit protection, and thermal shutdown. These provisions further enhance the reliability of the system solution.

The device is housed in a thermally enhanced 16 pin 3mmx3mm QFN package

2. FEATURES

- Input Voltage: 4.0V to 5.5V
- Integrated Full Bridge FETs and
- Drivers
- 20mohm Rds(on) of Each FET for High Efficiency
- FET Driver Optimized for Low EMI
- Integrated 2.5V LDO to Bias External Circuit
- High Accuracy, High Speed, Lossless Current Measurement
- Input Under-Voltage Lockout
- Short-Circuit Protection
- Thermal shutdown
- 3mm x 3mm Flip Chip QFN Package

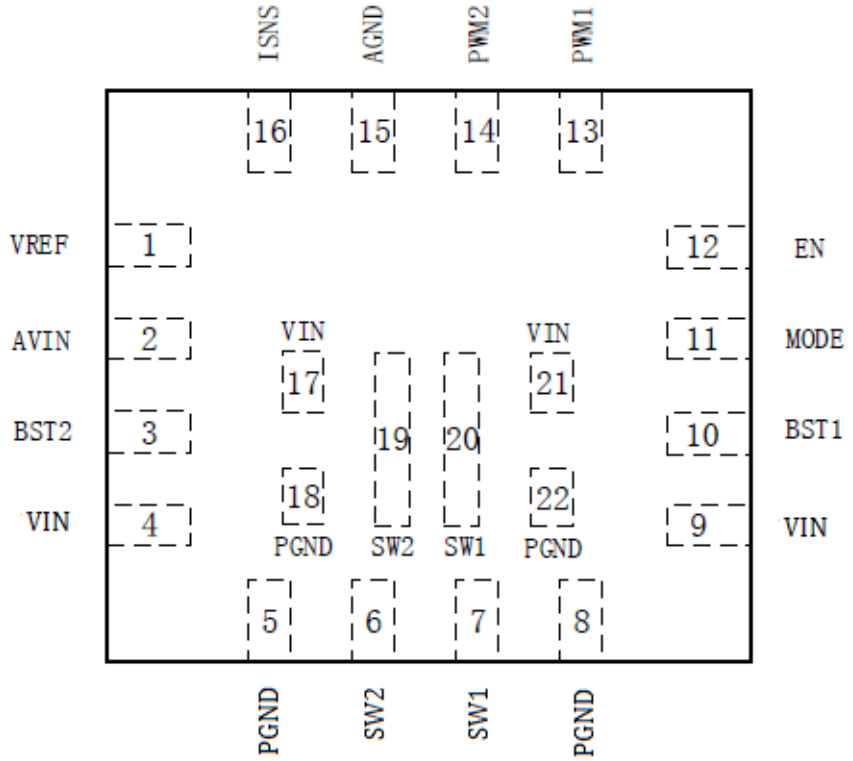
3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

NAME	PIN No.	Type	Description
VREF	1	O	This pin is the output of the 2.5V LDO
AVIN	2	I	Signal power input pin
BST2	3	I/O	Positive supply rail for the high-side gate driver of Q3 as shown in the **Block Diagram**. Connect a ceramic capacitor between the BST2 and SW2 pins
VIN	4,9,17,21	I	Power input pin. This pin connects to the input rail of the full bridge.
PGND	5,8,18,22	-	Power ground pin. This pin connects to the ground of the full bridge.
SW2	6,19	O	Switch node of the half-bridge MOSFETs Q3 and Q4, as shown in the **Block Diagram**.
SW1	7,20	O	Switch node of the half-bridge MOSFETs Q1 and Q2, as shown in the **Block Diagram**.
BST1	10	I/O	Positive supply rail for the high-side gate driver of Q1. Connect a ceramic capacitor between the BST1 and SW1 pins
MODE	11	I	The logic of the pin programs the PWM1 and PWM2 function. See **Application Description** for details. MODE logic is detected at power up, and will be reset at next power on set.
EN	12	I	Enable input of the IC. Pull the pin low or keep it floating to disable the IC and open all the FETs. Logic high enables the IC.
PWM1	13	I	PWM logic input to the MOSFET Q1 and Q2 as shown in the **Block Diagram**. Logic high turns on the high side FET, and turns off the low side FET. Logic low turns on the low side FET and turns off the high side FET. When PWM input is in the tri-state mode, both Q1 and Q2 are turned off. The switching slew rate and dead-time are controlled by the device.
PWM2	14	I	PWM logic input to the MOSFET Q3 and Q4 as shown in the **Block Diagram**. Logic high turns on the high side FET, and turns off the low side FET. Logic low turns on the low side FET and turns off the high side FET. When PWM input is in the tri-state mode, both Q3 and Q4 are turned off. The switching slew rate and dead-time are controlled by the device.
AGND	15	-	Analog ground of the IC
ISNS	16	O	Current sense output. When connected with an external resistor, the voltage at the pin represents the input current.

4.1. PIN Map



16-Pin QFN

Top View

5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
SW1, SW2	Switch node of the half-bridge MOSFETs Voltage.	-0.3 to 12	V
PWM1,PWM2, VREF,VIN, AVIN,EN, MODE,ISNS	Other General Pin Voltage.	-0.3 to 7	V
BST1	BST1 and SW1 pin Voltage	-0.3 to 7+SW1	V
BST2	BST2 and SW2 pin Voltage	-0.3 to 7+SW1	V
T_{stg}	Storage Temperature	-55 to +150	℃
T_J	Operating junction Temperature	-40 to 125	℃

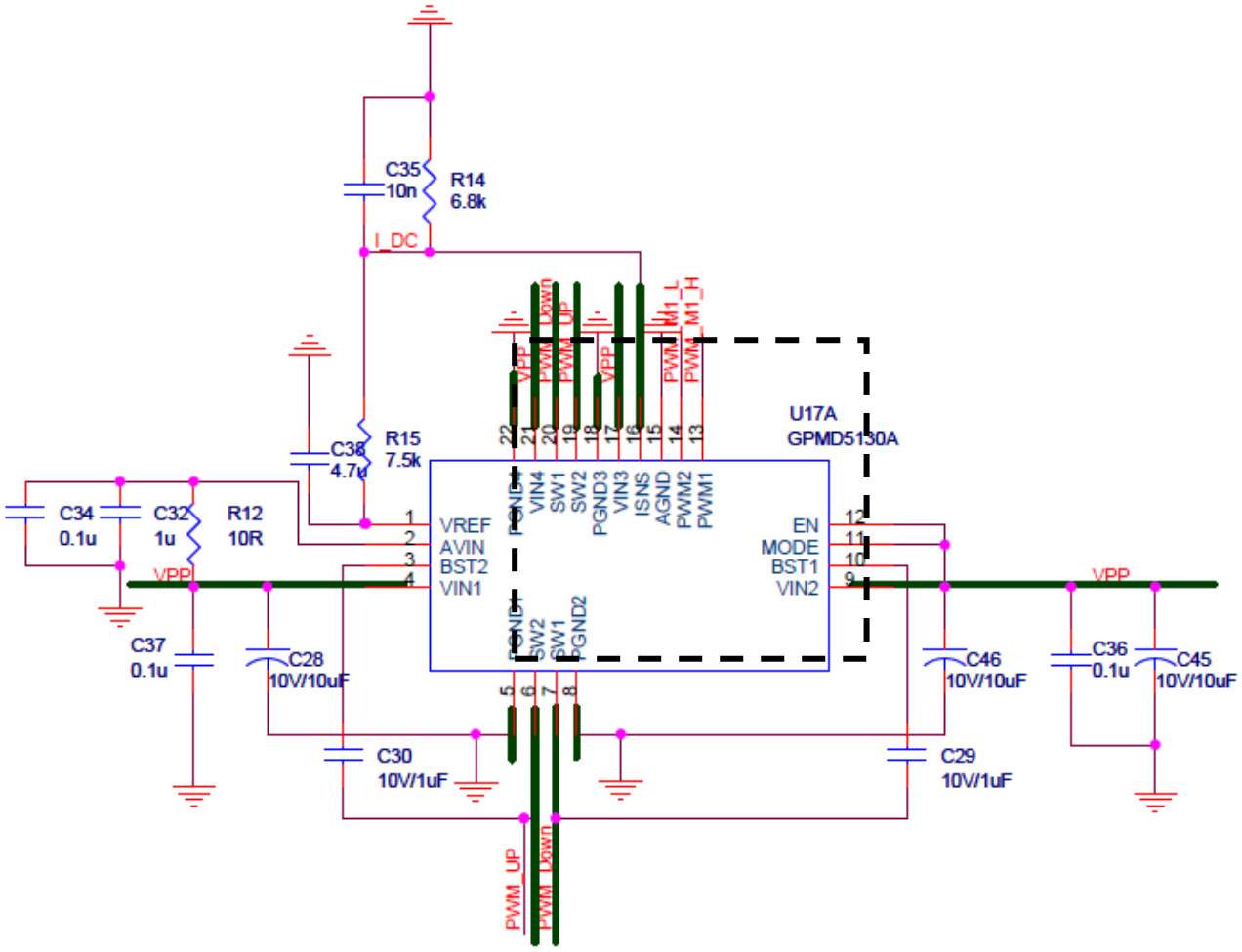
5.2. Electrical Characteristics

(VIN=AVIN=5V, Fsw=200KHz, Tj=-40℃ to 125℃ (unless otherwise noted))

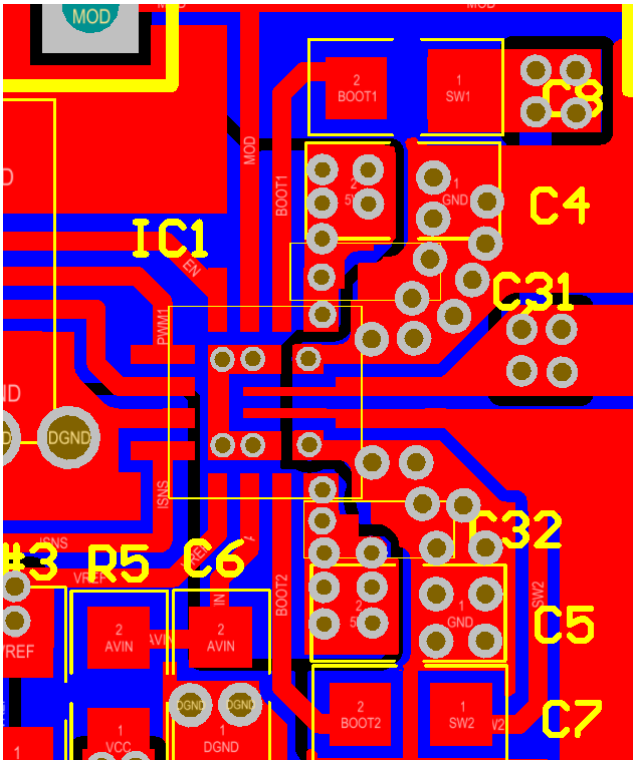
Symbol	Parameter	Test Conditions	GPMD5130A			Unit
			Min	Typ	Max	
INPUT						
VUVLO	Under voltage lock out threshold	AVIN ramps up	3.3	3.6	3.8	V
VUVLO_HYS	Under voltage lock out hysteresis voltage	AVIN ramps down	-	400	-	mV
IIN	Input operating current (IVIN+IAVIN)	No switching, EN=1	-	3	-	mA
ISD	Input shutdown current (IVIN+IAVIN)	Tj=-40℃ to 85℃, EN=0	-		1	uA
POWER DEVICES and DRIVERS						
RDS(on)	FET on resistance		-	20	-	mohm
ISW_LEAK	SW pin leakage current	VSW=5V and VIN floating or VSW=0V and VIN=5V	-1	-	1	uA
VBST_FW	Bootstrap forward voltage		-	-	500	mV
IBST_LEAK	Boot leakage current	VBST-VIN=5V	-	-	2	uA
PWM, MODE and ENABLE INPUTS						
VH	PWM logic high	Input rising	2.65	-	-	V
VL	PWM logic low	Input falling	-	-	0.6	V
VTRI	Tri state voltage	Input rising and falling	1.3	-	2	V
TACT	Tri state activation timing		-	100	-	ns
VEH, VMODEH	EN pin and MODE pin high	Input rising	2.65	-	-	V
VEL, VMODEL	EN pin and MODE pin low	Input falling	-	-	0.6	V
IPWM	PWM pin input bias current	VPWM=VIN, VPWM=GND	-	15	-	uA
REN	Enable pin input impedance	Pull down to GND	-	800	-	Kohm
REFERENCE OUTPUT						
VREF	2.5V reference voltage	Different temp, line and load.	-2%	2.5	+2%	V
IREF	Reference voltage maximum supply current		10	-		mA
PROTECTIONS						
TOTP	Over temperature protection point	Temp rising	-	155	-	℃
TOTP_HYS	Over temperature protection hysteresis	Temp rising and falling	-	30	-	℃
ISC	High side short circuit protection point		6	8	10	A
TSC	OC protection time out period		10	20	30	ms
Current Sense						

K_{sns}	current amplification factor, I_{vin}/ I_{sns}	I_{vin}=0.8A and I_{vin}=1.6A	6762	6900	7038	
I_{offset}	Current amplification offset, I_{sns} *K_{sns} -I_{vin}	I_{vin}=0.8A and I_{vin}=1.6A	-14.4	-	14.4	mA

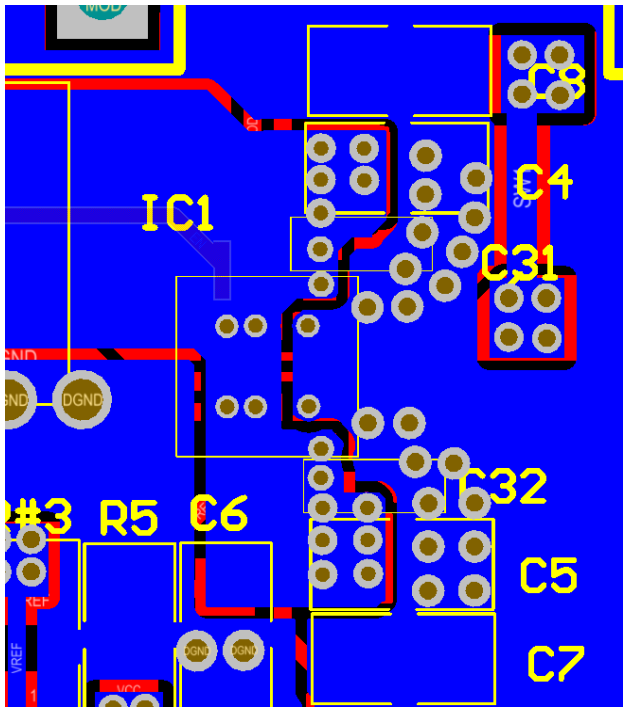
6. APPLICATION CIRCUIT



7. LAYOUT EXAMPLES



Top layer view



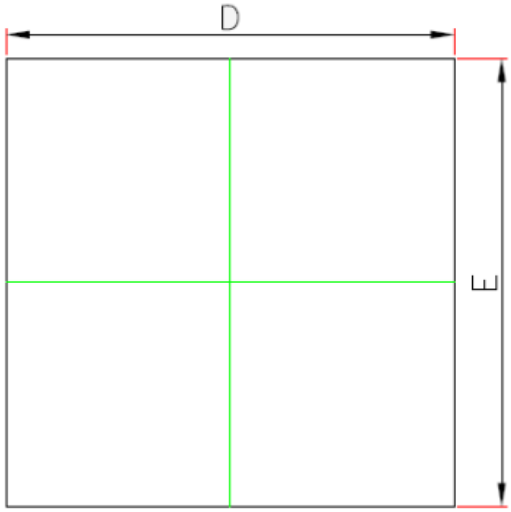
Bottom layer view

8. PACKAGE / ORDERING INFORMATION

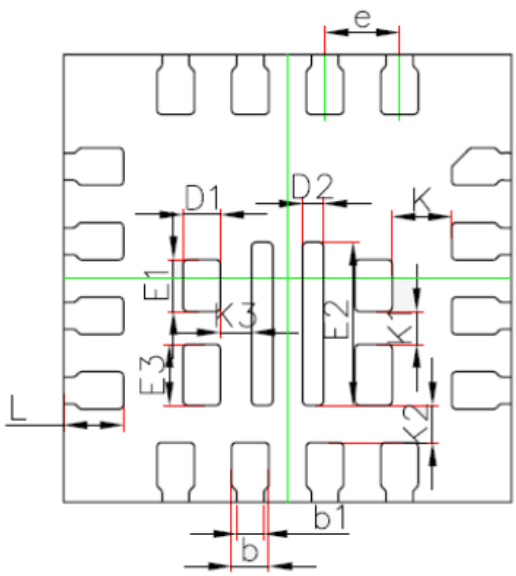
8.1. Ordering Information

Product Number	Package Type
GPMD5130A	QFN16

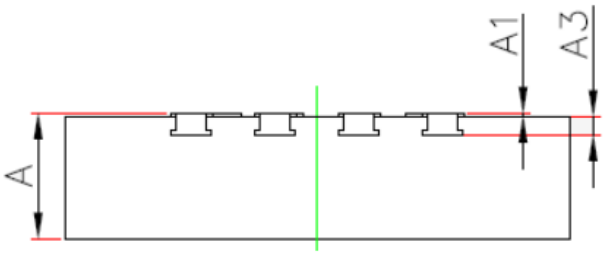
8.2. Package Information



Top view



Bottom view



Side view

Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.004	0.021	0.046	0.000	0.001	0.002
A3	0.110 REF.			0.004 REF.		
D	0.29	0.30	0.31	0.114	0.118	0.122
D1	0.15	0.25	0.35	0.006	0.01	0.014
E	2.9	3.0	3.1	0.114	0.118	0.122
E1	0.248	0.348	0.448	0.01	0.014	0.018

D2	0.041	0.141	0.241	0.002	0.0055	0.009
E2	0.993	1.093	1.193	0.039	0.043	0.047
E3	0.309	0.409	0.509	0.012	0.016	0.02
b	0.2	0.25	0.3	0.08	0.1	0.012
b1	0.13	0.18	0.23	0.05	0.07	0.09
e	0.5 TYP			0.02 TYP		
L	0.3	0.4	0.5	0.012	0.016	0.02
k	0.399REF			0.016REF		
k1	0.220REF			0.009REF		
k2	0.250REF			0.010REF		
k3	0.210REF			0.008REF		

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
JUNE. 7, 2016	1.0	Original	